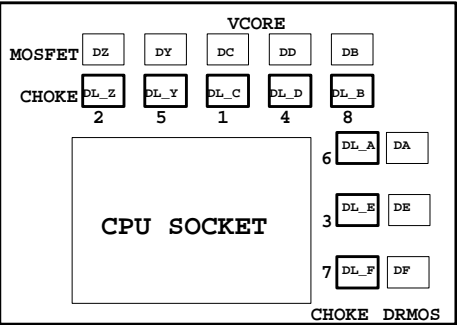


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	DVI / DP
15	HDMI / SPDIF
16	PCI EXPRESS*1 SLOTS X3
17	Dual BIOS
18	Realtek ALC1150
19	REAR AUDIO JACK
20	IR3580 PWM
21	IR3598-VCORE
22	IR3570_DDR PWM
23	IR3598-DDR
24	DISCRETE POWER I
25	DISCRETE POWER II
26	I/O ITE8620
27	FP,F_USB,USB PWR,FDD,BZ,TB_C, COMA
28	USB DAC-UP , PS2
29	ATX POWER
30	RST, PWR, CLR_CMOS, 80 PORT
31	LAN E2201
32	R_USB30
33	RENESAS USB3 HUB-1
34	RENESAS USB3 HUB-1

35	F_USB3.0 , SATA EXPRESS
36	IT8790
37	FAN CTRL
38	PCIEx16(x8) REFCLK
39	PCI EXPRESS*16_2 SLOT
40	PCI EXPRESS X16 SWITCH_2
41	PCI EXPRESS*8_2 SLOT
42	PCI EXPRESS*16_1 SLOT
43	PCI EXPRESS X16 SWITCH_1
44	PCI EXPRESS*8_1 SLOT
45	PEX8747S UPSTREAM & MISC
46	PEX8747S DOWNSTREAM SLOTS
47	PEX8747S STRAP & CPLD INTF
48	PEX8747S POWER
49	PEX8747 POWER DESIGN
50	Marvell 9172 1
51	TABLE LIST



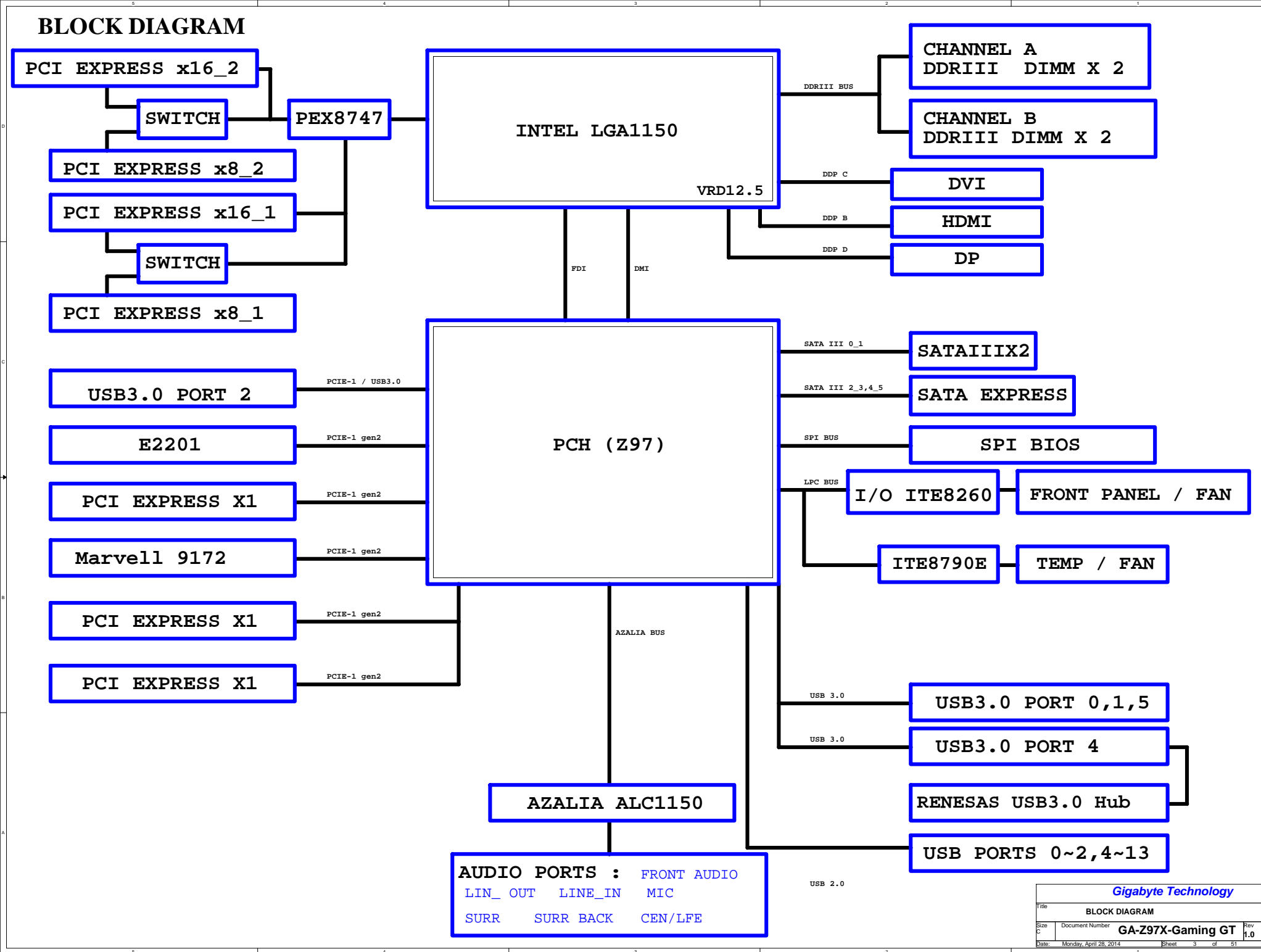
## Component value change history

[illegible][illegible]

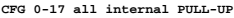
Circuit or PCB layout change

[illegible]

# BLOCK DIAGRAM



(E)



(D)



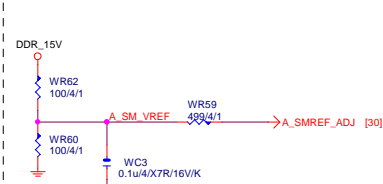
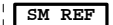
(C)



**-CPURST**



CPU\_VTT\_OR



## CPU LGA1150-A

Size Custom	Document Number <b>GA-Z97X-Gaming GT</b>	Rev 1.0
Date: Monday, April 28, 2014	Sheet 4 of 51	

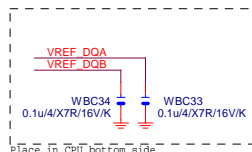
LGA1150A

MAAA0	AU13	DDR0_MA0	DDR0_DQ0	AD38	MDA0
MAAA1	AV16	DDR0_MA1	DDR0_DQ1	AD39	MDA1
MAAA2	AU16	DDR0_MA2	DDR0_DQ2	AF38	MDA2
MAAA3	AW17	DDR0_MA3	DDR0_DQ3	AF39	MDA3
MAAA4	AU17	DDR0_MA3	DDR0_DQ3	AD37	MDA4
MAAA5	AW18	DDR0_MA4	DDR0_DQ4	AD40	MDA5
MAAA6	AV17	DDR0_MA5	DDR0_DQ5	AF37	MDA6
MAAA7	AT18	DDR0_MA6	DDR0_DQ6	AF40	MDA7
MAAA8	AU18	DDR0_MA7	DDR0_DQ7	AF40	MDA9
MAAA9	AT19	DDR0_MA8	DDR0_DQ8	AD39	MDA13
MAAA10	AW11	DDR0_MA9	DDR0_DQ9	AK38	MDA10
MAAA11	AV19	DDR0_MA10	DDR0_DQ10	AK39	MDA11
MAAA12	AU19	DDR0_MA11	DDR0_DQ11	AH37	MDA12
MAAA13	AY10	DDR0_MA12	DDR0_DQ12	AH38	MDA8
MAAA14	AT20	DDR0_MA13	DDR0_DQ13	AK37	MDA14
MAAA15	AU21	DDR0_MA14	DDR0_DQ14	AK40	MDA15
		DDR0_MA15	DDR0_DQ15	AK40	MDA17
MODT_A0	AW10	DDR0_ODT0	DDR0_DQ16	AM40	MDA17
MODT_A1	AY8	DDR0_ODT1	DDR0_DQ17	AM39	MDA21
MODT_A2	AW9	DDR0_ODT2	DDR0_DQ18	AP38	MDA18
MODT_A3	AU8	DDR0_ODT3	DDR0_DQ19	AP39	MDA19
			DDR0_DQ20	AM37	MDA20
			DDR0_DQ21	AM38	MDA16
			DDR0_DQ22	AP37	MDA22
			DDR0_DQ23	AP40	MDA23
			DDR0_DQ24	AV37	MDA25
			DDR0_DQ25	AV37	MDA29
			DDR0_DQ26	AU35	MDA26
			DDR0_DQ27	AV35	MDA27
			DDR0_DQ28	AT37	MDA28
			DDR0_DQ29	AU37	MDA24
			DDR0_DQ30	AT35	MDA30
			DDR0_DQ31	AW35	MDA31
			DDR0_DQ32	AM38	MDA37
			DDR0_DQ33	AU6	MDA34
			DDR0_DQ34	AU4	MDA35
			DDR0_DQ35	AW6	MDA36
			DDR0_DQ36	AV6	MDA32
			DDR0_DQ37	AW4	MDA38
			DDR0_DQ38	AY4	MDA39
			DDR0_DQ39	AR1	MDA41
			DDR0_DQ40	AR4	MDA45
			DDR0_DQ41	AN3	MDA42
			DDR0_DQ42	AN4	MDA43
			DDR0_DQ43	AR2	MDA44
			DDR0_DQ44	AR3	MDA40
			DDR0_DQ45	AN2	MDA46
			DDR0_DQ46	AN1	MDA47
			DDR0_DQ47	AL1	MDA49
			DDR0_DQ48	AL4	MDA53
			DDR0_DQ49	AJ3	MDA50
			DDR0_DQ50	AJ4	MDA51
			DDR0_DQ51	AL2	MDA52
			DDR0_DQ52	AL3	MDA48
			DDR0_DQ53	AJ2	MDA54
			DDR0_DQ54	AJ1	MDA55
			DDR0_DQ55	AG1	MDA57
			DDR0_DQ56	AG4	MDA61
			DDR0_DQ57	AE3	MDA58
			DDR0_DQ58	AE4	MDA59
			DDR0_DQ59	AG2	MDA60
			DDR0_DQ60	AG3	MDA56
			DDR0_DQ61	AE2	MDA62
			DDR0_DQ62	AE1	MDA63
			DDR0_DQ63	AE39	DQSA0
			DDR0_DQ64	AJ39	DQSA1
			DDR0_DQ65	AN39	DQSA2
			DDR0_DQ66	AV36	DQSA3
			DDR0_DQ67	AV5	DQSA4
			DDR0_DQ68	AP3	DQSA5
			DDR0_DQ69	AK3	DQSA6
			DDR0_DQ70	AF3	DQSA7
			DDR0_DQ71	AV32	DQSA0
			DDR0_DQ72	AE38	DQSA1
			DDR0_DQ73	AJ38	DQSA2
			DDR0_DQ74	AN38	DQSA3
			DDR0_DQ75	AU36	DQSA4
			DDR0_DQ76	AW5	DQSA5
			DDR0_DQ77	AP2	DQSA6
			DDR0_DQ78	AK2	DQSA7
			DDR0_DQ79	AF2	DQSA7
			DDR0_DQ80	AU32	

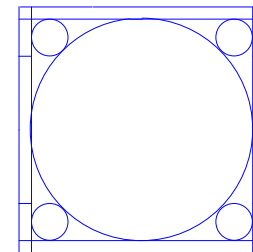
HASWELL[10SC1-F01150-01R]

LGA1150B

MAAB0	AL19	DDR1_MA0	DDR1_DQ0	AE34	MDB0
MAAB1	AK23	DDR1_MA1	DDR1_DQ1	AE35	MDB1
MAAB2	AM22	DDR1_MA2	DDR1_DQ2	AG35	MDB2
MAAB3	AM23	DDR1_MA3	DDR1_DQ3	AH35	MDB3
MAAB4	AP23	DDR1_MA4	DDR1_DQ4	AD34	MDB4
MAAB5	AL23	DDR1_MA5	DDR1_DQ5	AD35	MDB5
MAAB6	AY24	DDR1_MA6	DDR1_DQ6	AG34	MDB6
MAAB7	AV25	DDR1_MA7	DDR1_DQ7	AH34	MDB7
MAAB8	AU25	DDR1_MA8	DDR1_DQ8	AL34	MDB8
MAAB9	AW25	DDR1_MA9	DDR1_DQ9	AK35	MDB9
MAAB10	AP18	DDR1_MA10	DDR1_DQ10	AK31	MDB10
MAAB11	AY25	DDR1_MA11	DDR1_DQ11	AL31	MDB11
MAAB12	AV26	DDR1_MA12	DDR1_DQ12	AK34	MDB12
MAAB13	AR15	DDR1_MA13	DDR1_DQ13	AK35	MDB13
MAAB14	AV27	DDR1_MA14	DDR1_DQ14	AK32	MDB14
MAAB15	AY28	DDR1_MA15	DDR1_DQ15	AL32	MDB15
			DDR1_DQ16	AN34	MDB17
			DDR1_DQ17	AP34	MDB21
			DDR1_DQ18	AN31	MDB19
			DDR1_DQ19	AP31	MDB23
			DDR1_DQ20	AN35	MDB20
			DDR1_DQ21	AP35	MDB18
			DDR1_DQ22	AN32	MDB19
			DDR1_DQ23	AP32	MDB22
			DDR1_DQ24	AM29	MDB25
			DDR1_DQ25	AM28	MDB28
			DDR1_DQ26	AR29	MDB27
			DDR1_DQ27	AR28	MDB30
			DDR1_DQ28	AL29	MDB24
			DDR1_DQ29	AL28	MDB29
			DDR1_DQ30	AP29	MDB26
			DDR1_DQ31	AP28	MDB31
			DDR1_DQ32	AR12	MDB32
			DDR1_DQ33	AP12	MDB33
			DDR1_DQ34	AL13	MDB34
			DDR1_DQ35	AL12	MDB35
			DDR1_DQ36	AR13	MDB36
			DDR1_DQ37	AP13	MDB37
			DDR1_DQ38	AM13	MDB38
			DDR1_DQ39	AM12	MDB39
			DDR1_DQ40	AR9	MDB45
			DDR1_DQ41	AP9	MDB41
			DDR1_DQ42	AR6	MDB47
			DDR1_DQ43	AP6	MDB43
			DDR1_DQ44	AR10	MDB44
			DDR1_DQ45	AP10	MDB40
			DDR1_DQ46	AR7	MDB46
			DDR1_DQ47	AP7	MDB42
			DDR1_DQ48	AM9	MDB52
			DDR1_DQ49	AL9	MDB53
			DDR1_DQ50	AL6	MDB50
			DDR1_DQ51	AL7	MDB55
			DDR1_DQ52	AM10	MDB48
			DDR1_DQ53	AM6	MDB54
			DDR1_DQ54	AM7	MDB51
			DDR1_DQ55	AH6	MDB61
			DDR1_DQ56	AH7	MDB60
			DDR1_DQ57	AE5	MDB59
			DDR1_DQ58	AE7	MDB63
			DDR1_DQ59	AJ6	MDB56
			DDR1_DQ60	AJ7	MDB57
			DDR1_DQ61	AF6	MDB58
			DDR1_DQ62	AF7	MDB62
			DDR1_DQ63	AF35	DQSB0
			DDR1_DQ64	AL33	DQSB1
			DDR1_DQ65	AN33	DQSB2
			DDR1_DQ66	AN29	DQSB3
			DDR1_DQ67	AN13	DQSB4
			DDR1_DQ68	AR8	DQSB5
			DDR1_DQ69	AM8	DQSB6
			DDR1_DQ70	AG6	DQSB7
			DDR1_DQ71	AN25	
			DDR1_DQ72	AF34	DQSB0
			DDR1_DQ73	AK33	DQSB1
			DDR1_DQ74	AN33	DQSB2
			DDR1_DQ75	AN29	DQSB3
			DDR1_DQ76	AN13	DQSB4
			DDR1_DQ77	AR8	DQSB5
			DDR1_DQ78	AM8	DQSB6
			DDR1_DQ79	AG6	DQSB7
			DDR1_DQ80	AN25	



HASWELL[10SC1-F01150-01R]

LGA1150  
ILM\_BP/1156/BKN[12KRC-0F0001-61R]

Need check the new CPU ME

DDR BUS

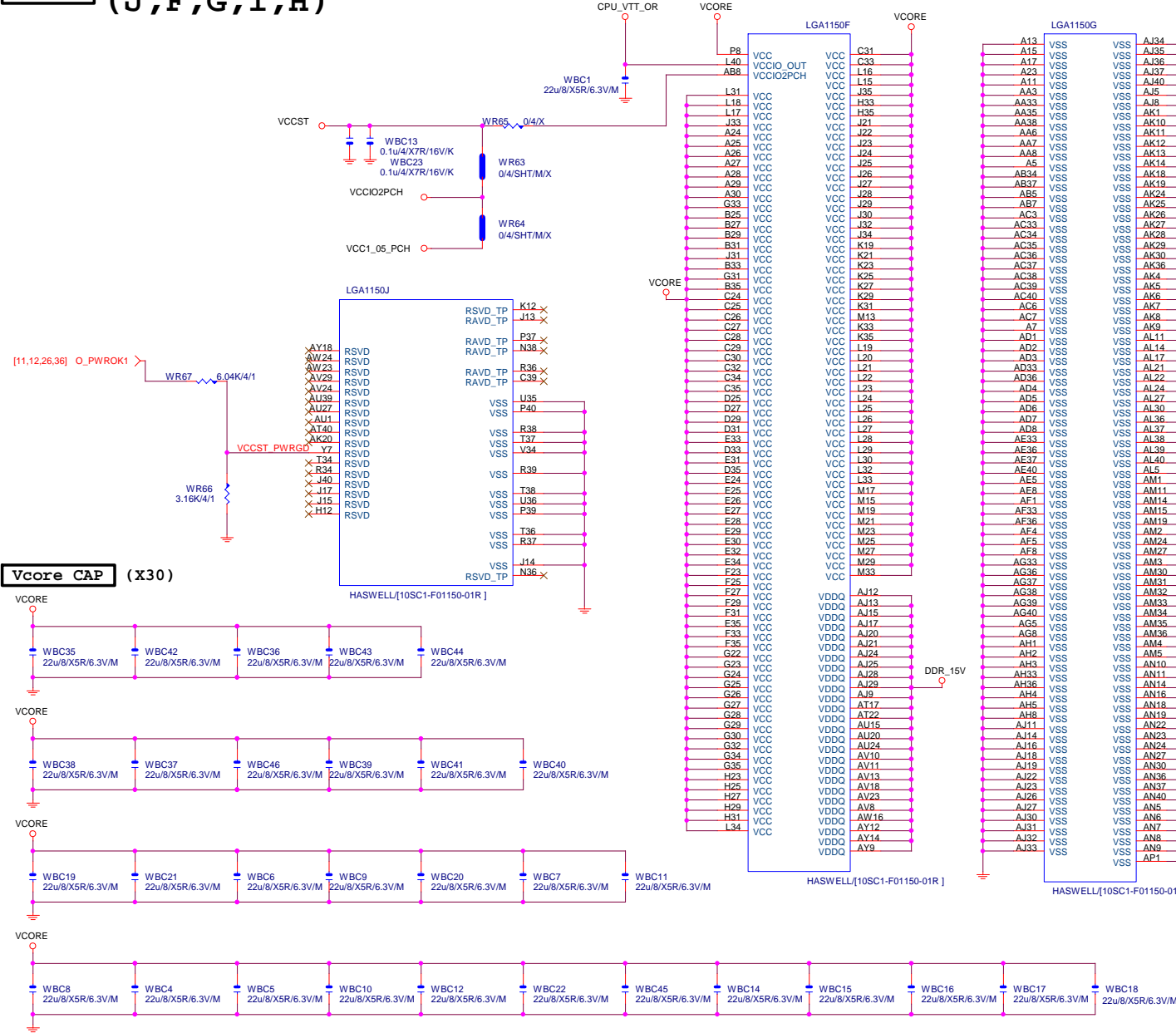
[7]	MODT_A[0..3]	←	MODT_A[0..3]
[8]	MODT_B[0..3]	←	MODT_B[0..3]
[7]	MDA[0..63]	←	MDA[0..63]
[8]	MDB[0..63]	←	MDB[0..63]
[7]	DQSA[0..7]	←	DQSA[0..7]
[7]	-DQSA[0..7]	←	-DQSA[0..7]
[7]	MAAA[0..15]	←	MAAA[0..15]
[8]	MAAB[0..15]	←	MAAB[0..15]
[8]	DQSB[0..7]	←	DQSB[0..7]
[8]	-DQSB[0..7]	←	-DQSB[0..7]

Gigabyte Technology

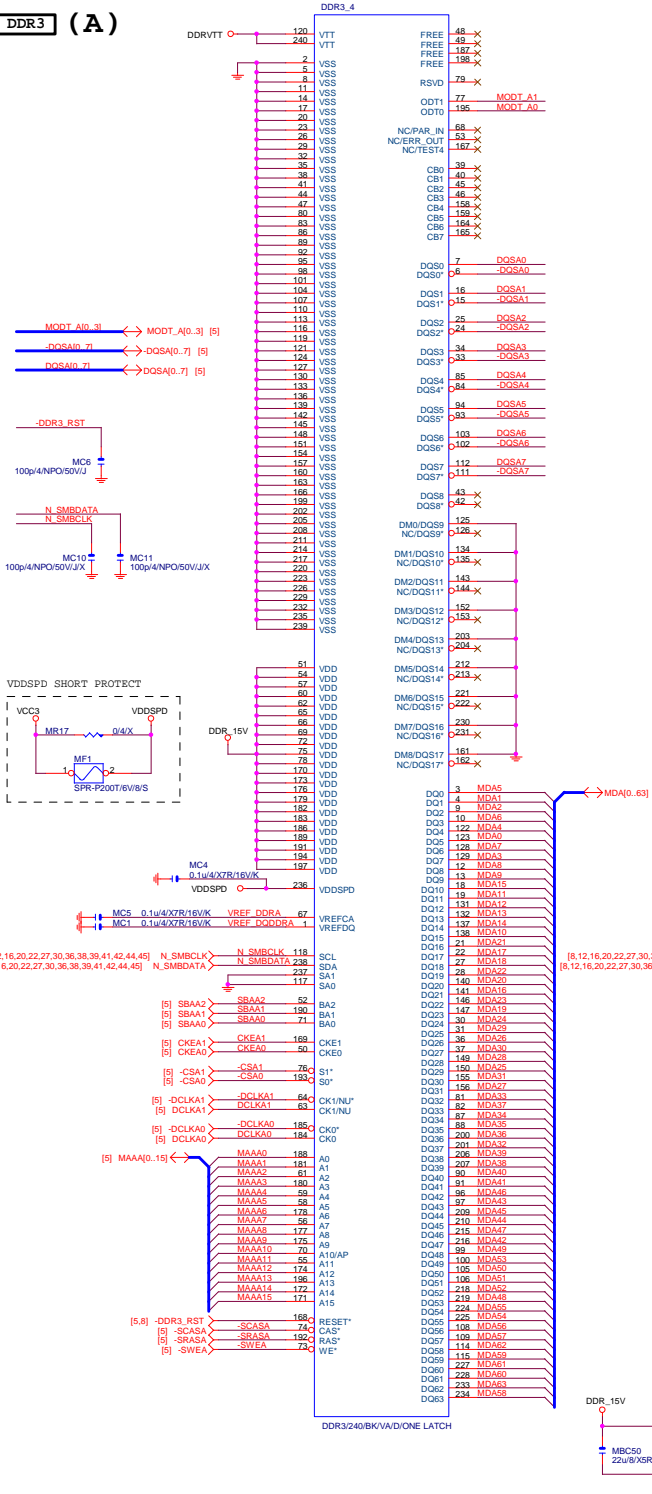
Title			CPU LGA1150-B		
Size	Document Number				Rev
Custom					
Date:			Monday, April 28, 2014		
Sheet			5 of 51		

GA-Z97X-Gaming G10

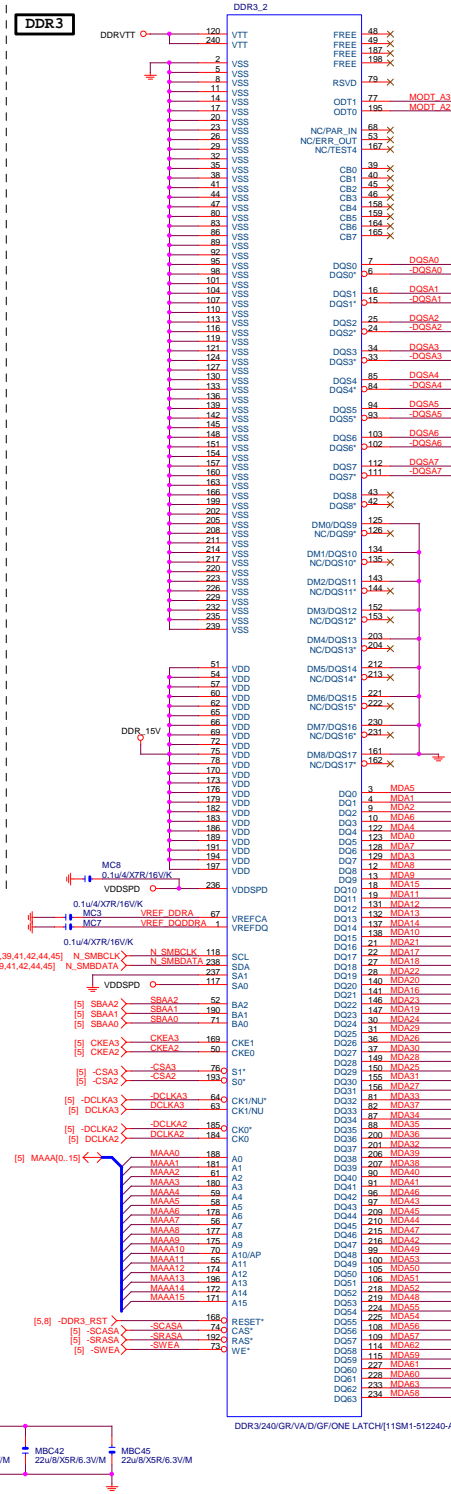
# LGA1150 (J,F,G,I,H)



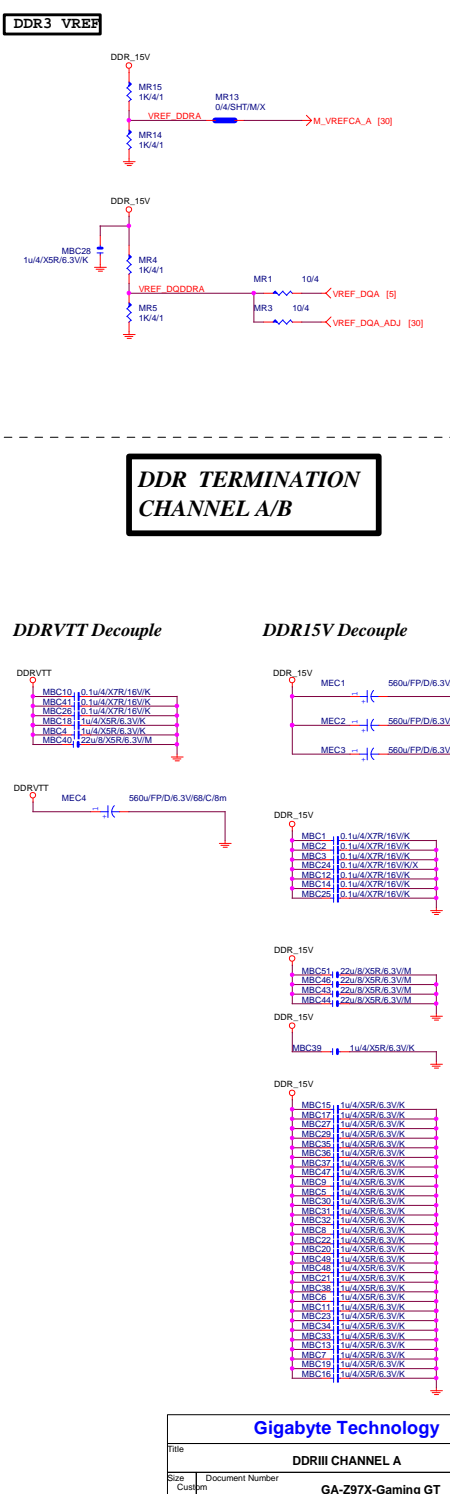
DDR3 (A)



DDR3

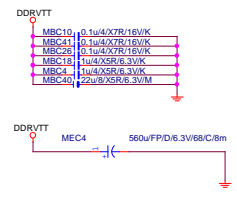


DDR3 VREF

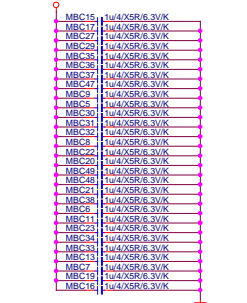
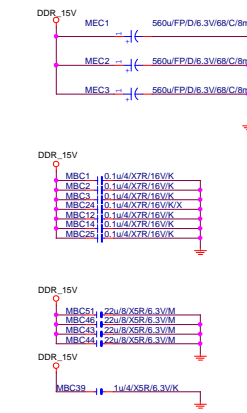


DDR TERMINATION CHANNEL A/B

DDRVTT Decouple



DDR15V Decouple



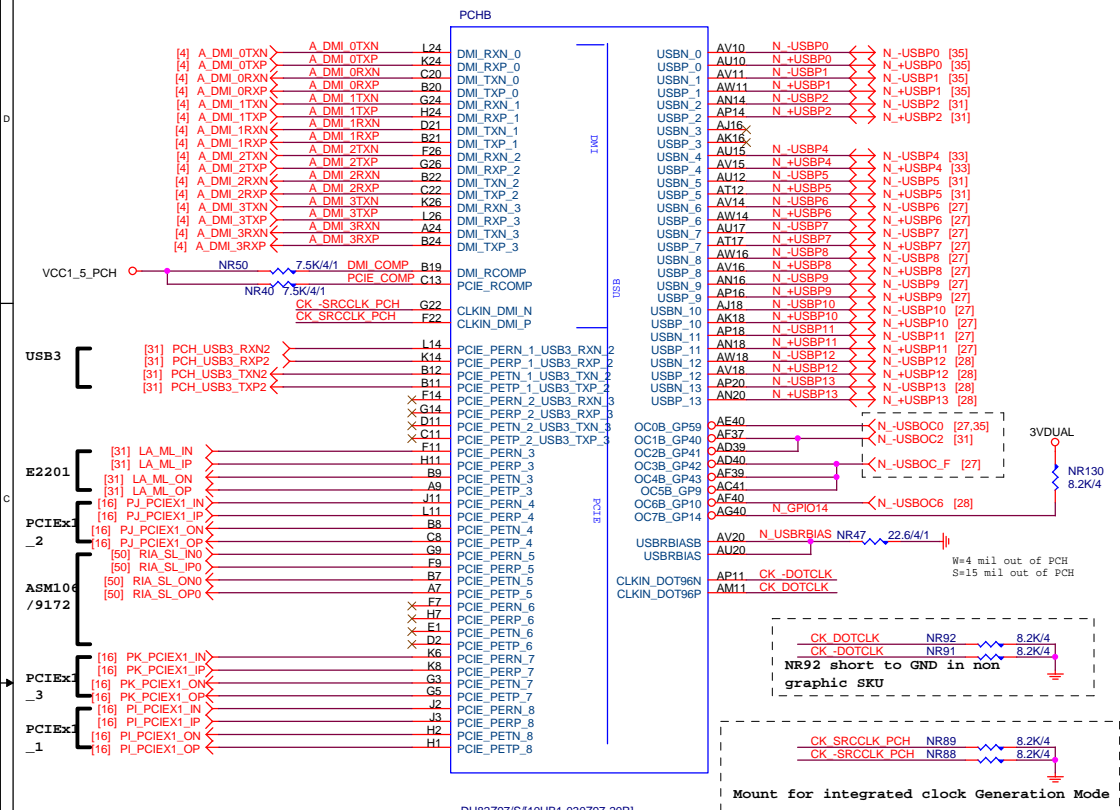
Gigabyte Technology		
Title		
DDR3 CHANNEL A		
Size		
Custom		
GA-Z97X-Gaming GT		
Date		
Sheet 7 of 51		
Rev 1.0		



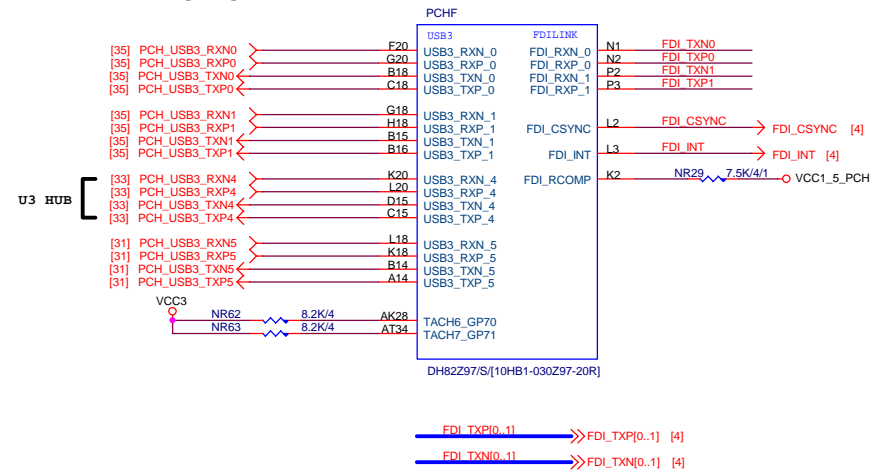




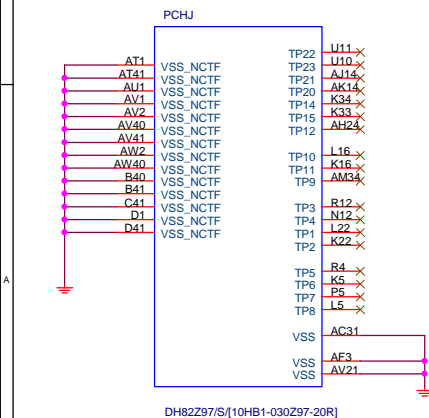
**PCH (B)**



**PCH (F)**



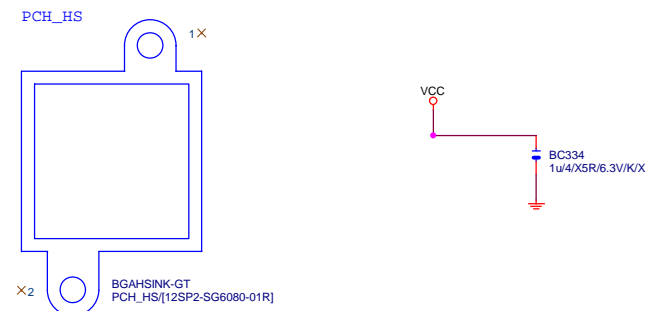
**PCH (J)**



## USB TABLE

OC[3:0]# for Device 29 (ports 0-7)													
OC[7:4]# for Device 26 (ports 8-13)													
USB3	00	01	02	05							04		
USB2	00	01	02	05	06	07	08	09	10	11	12	13	04
OCB0	OC0 (N_USBOC0)		OC1,2 (N_USBOC2)		OC3,4,5 (N_USBOC_F)				OC6 (N_USBOC6)		NA (Hub)		
Location	F_USB30		USB30_LAN		F_USB1 F_USB2 F_USB3				KB_USB		R_USB30		
Front/Rear	Front		Rear		Front				Rear		Rear		

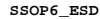
## PCH Heatsink



**(E)**



## VGA ESD



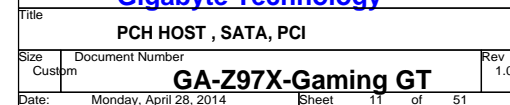
## VGA DDC

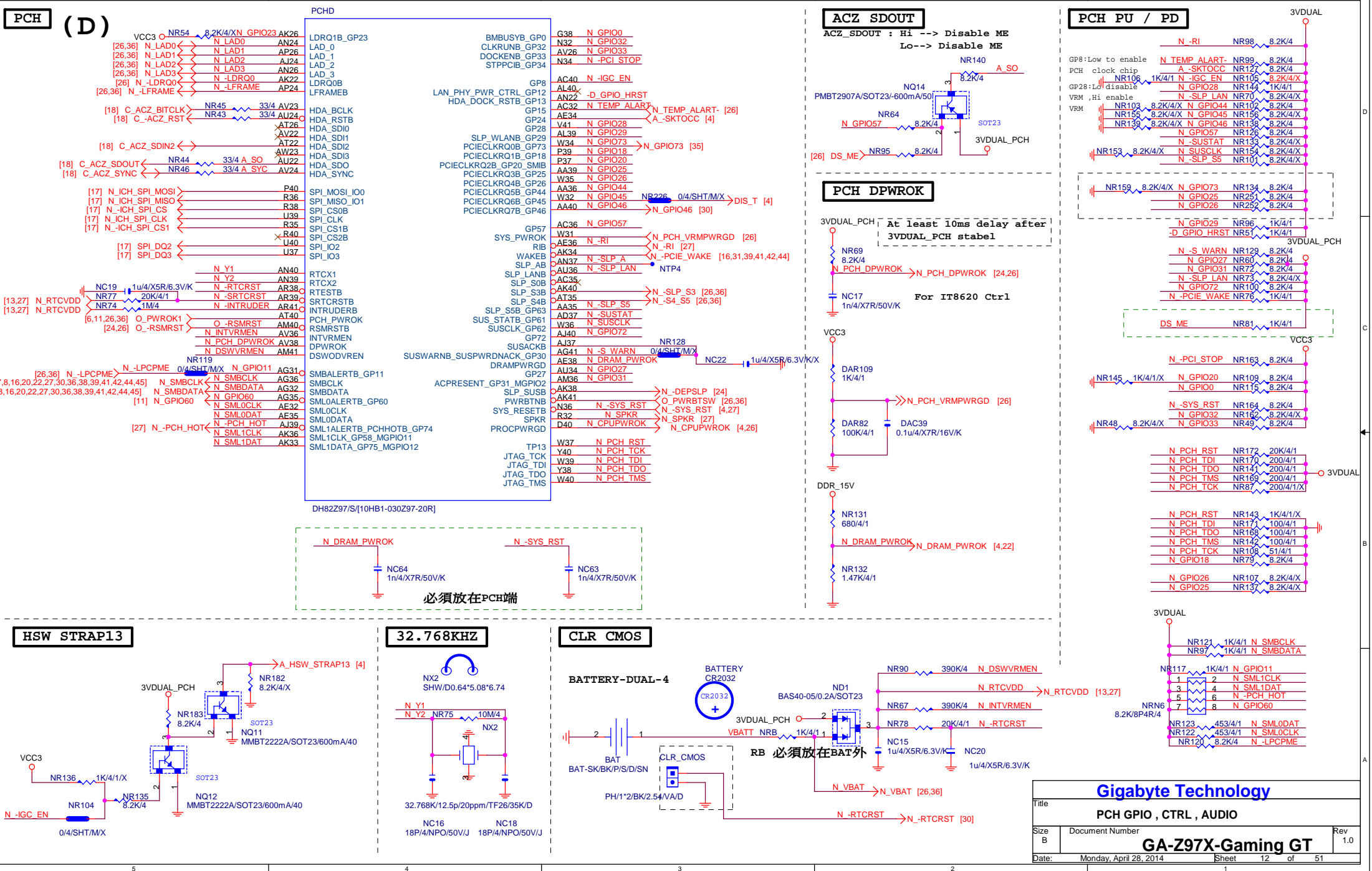


## VGA CONNECTOR

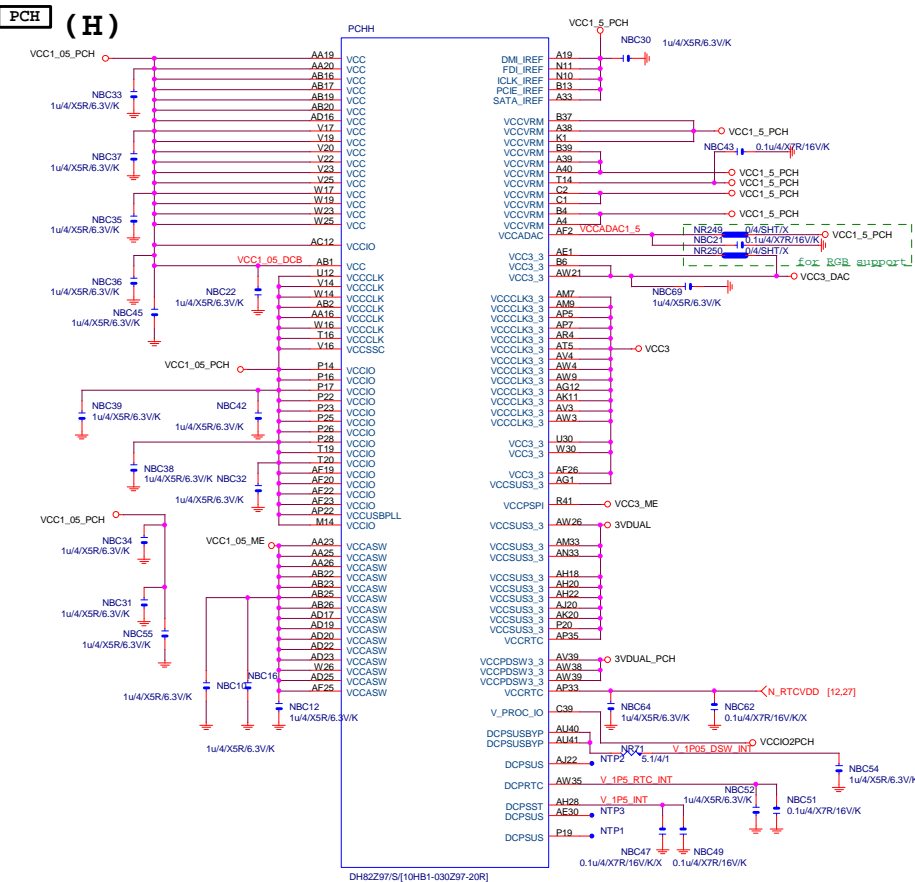
1

## PCH

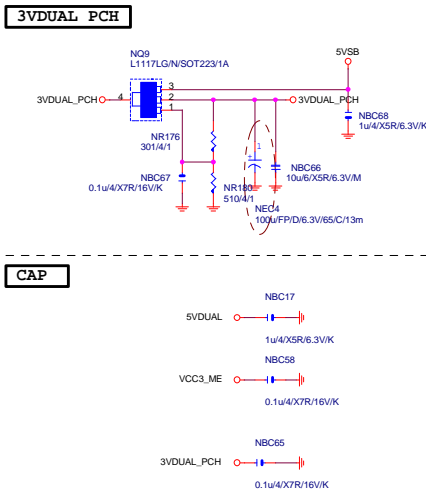




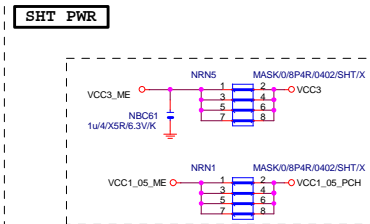
**PCH (H)**



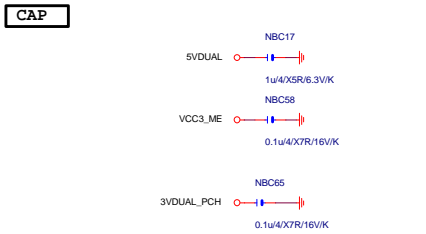
## 3VDUAL PCH



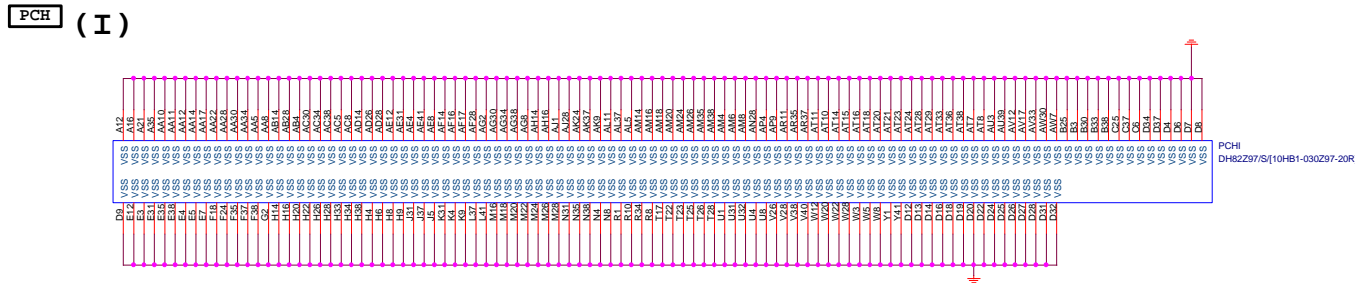
SHT PWR

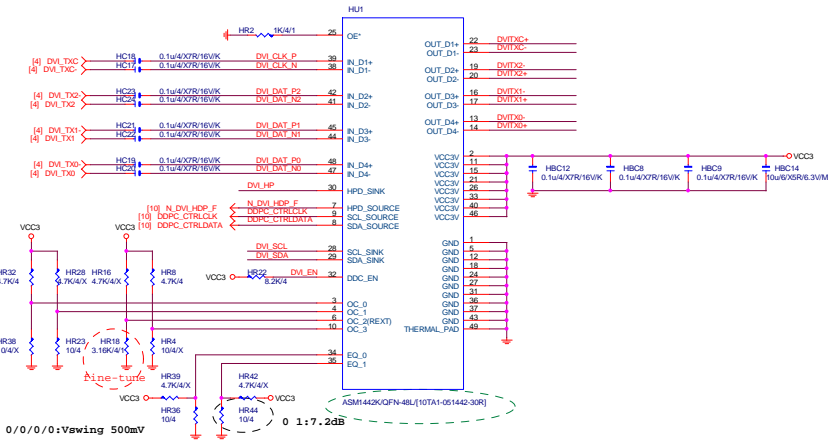


## CAP

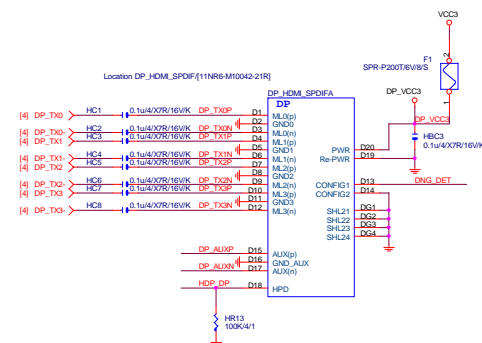
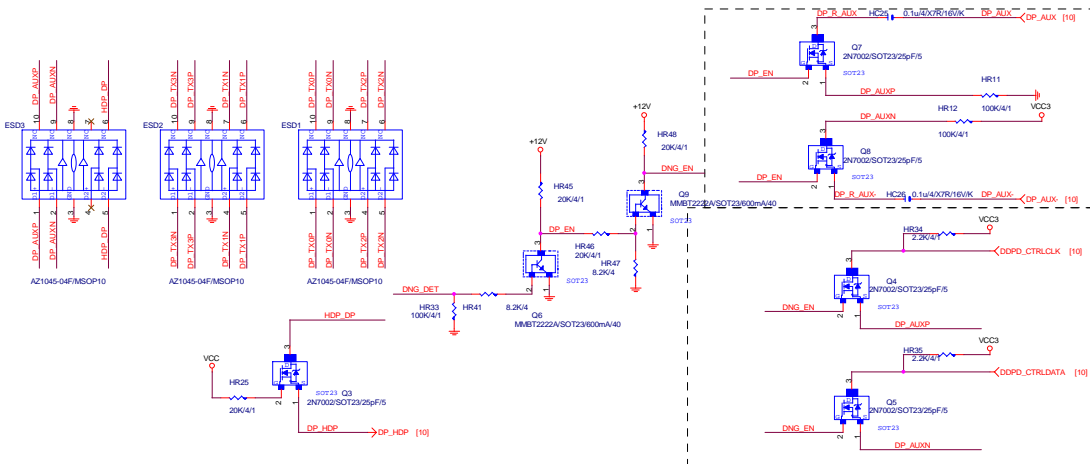
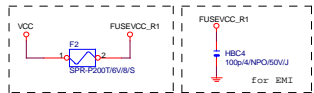
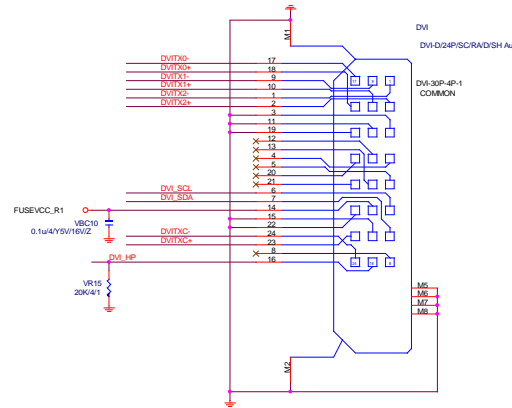
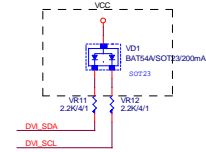


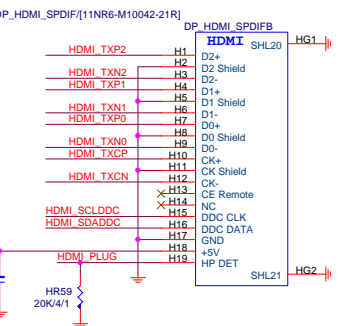
**PCH (I)**





# R&D技術通報 162

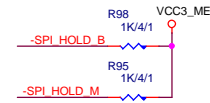
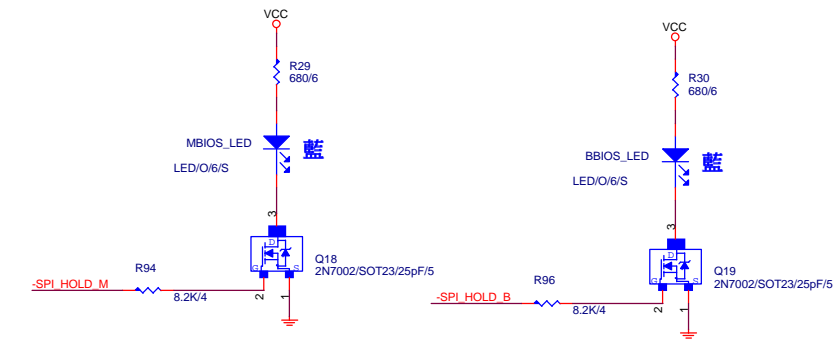




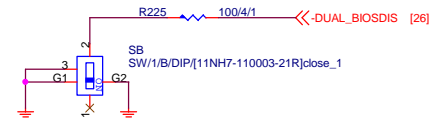
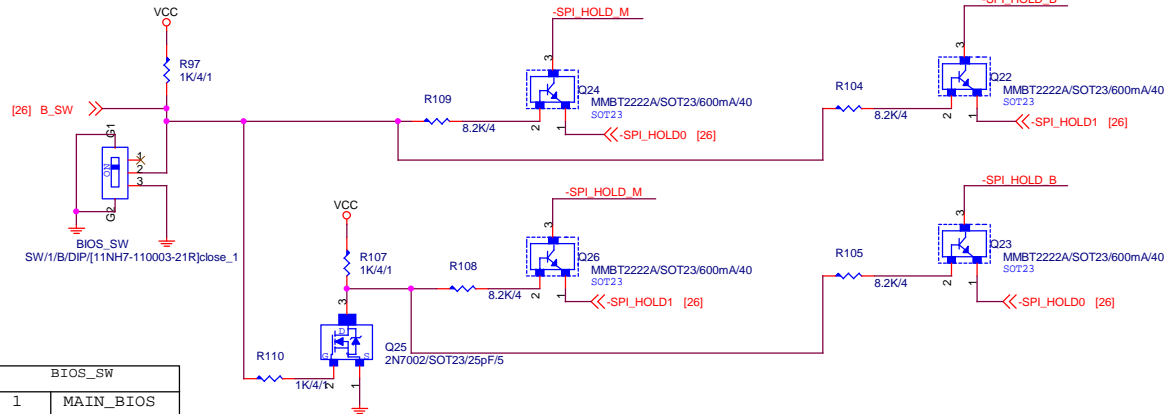
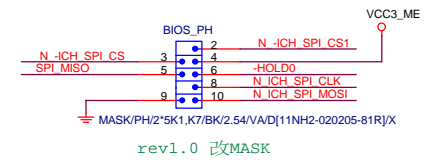
<b><i>Gigabyte Technology</i></b>				
Title				
<b>USB3 / HDMI</b>				
Size	Document Number	<b>GA-Z97X-Gaming G</b>		<b>Rev. 1.0</b>
Customer				
Date:	Monday, April 28, 2014	Sheet	15 of	51







### BIOS Debug port

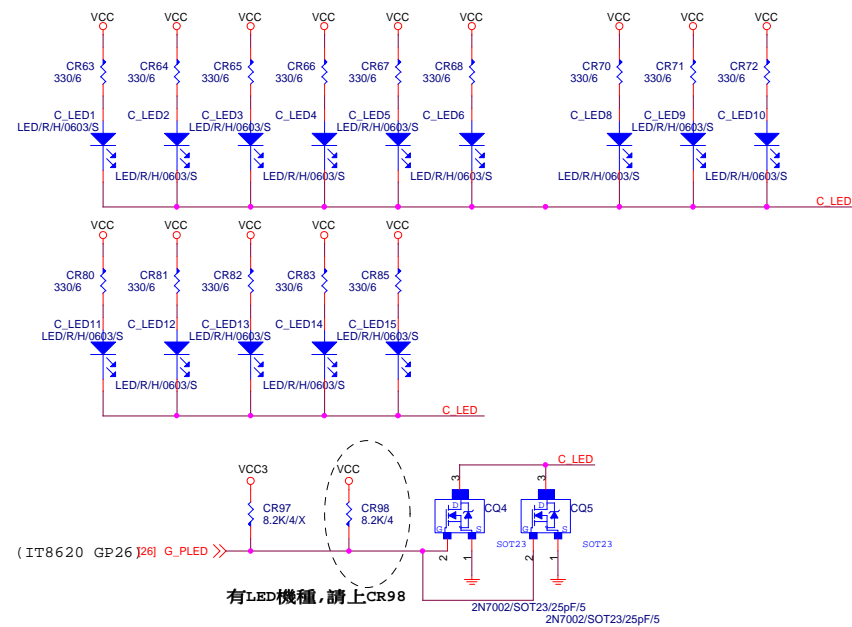
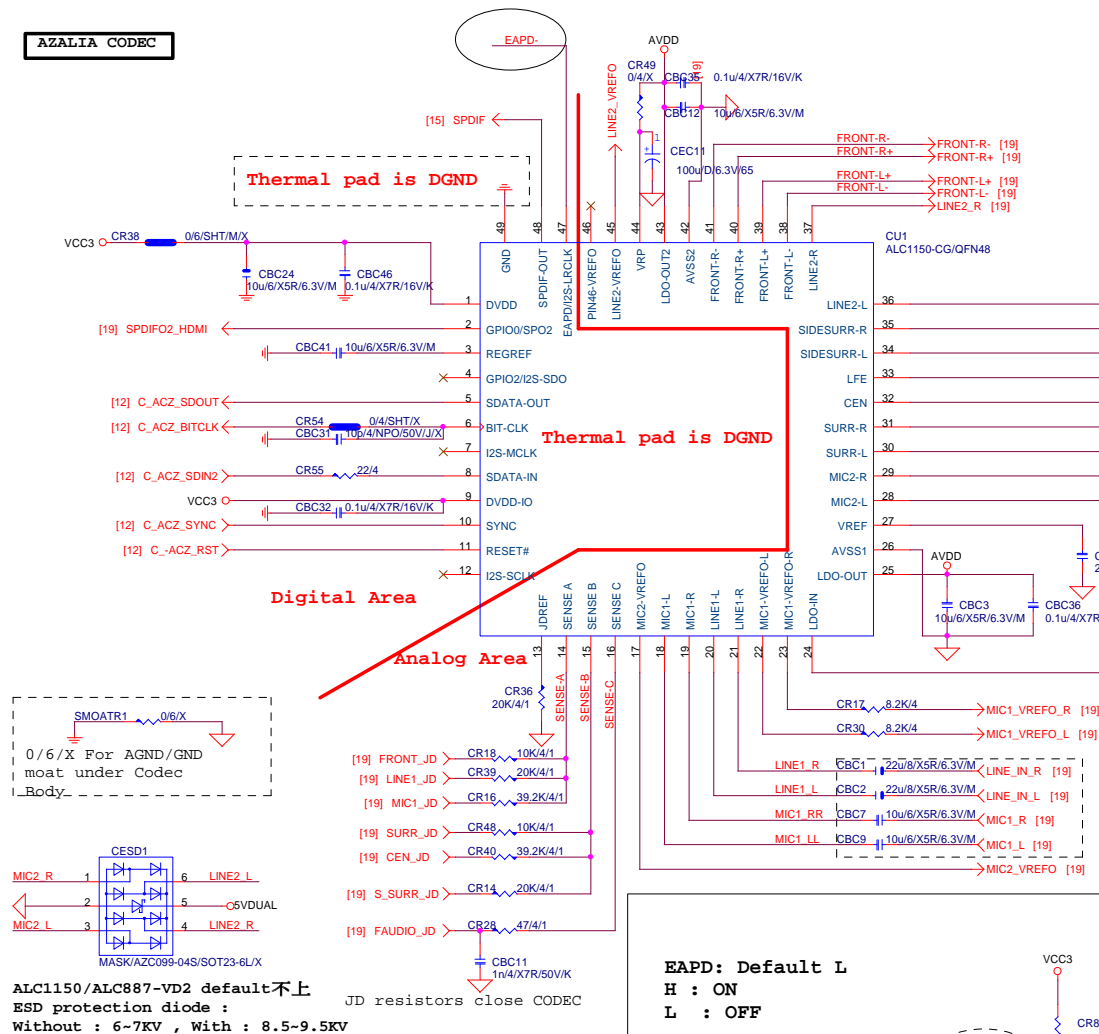


SB: SINGLE BIOS	
1	DISABLE
2	ENABLE

BIOS_SW	
1	MAIN_BIOS
2	BACKUP_BIOS

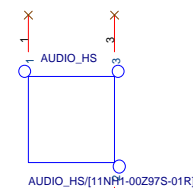
Gigabyte Technology	
Title: Dual BIOS	
Size Custom	Document Number: GA-Z97X-Gaming G1
Date: Monday, April 28, 2014	Sheet 17 of 51

# AZALIA CODEC

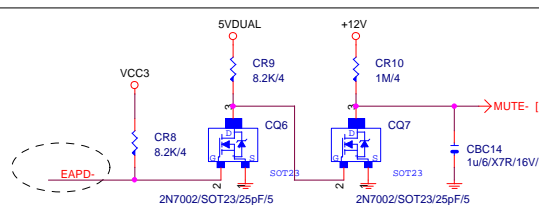


- BOM OPTION :**
1. 台固/日固/日黑固/MUSE MW音效電容
  2. 金屬外罩 Reserve
  3. LED Reserve (若LED有上, G\_PLED p-up請上CR98)

**ALC1150 "CD1" 惠謀指定default要上**



**金屬外罩+ GND切割**



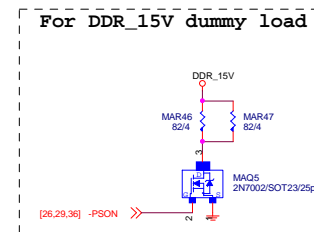
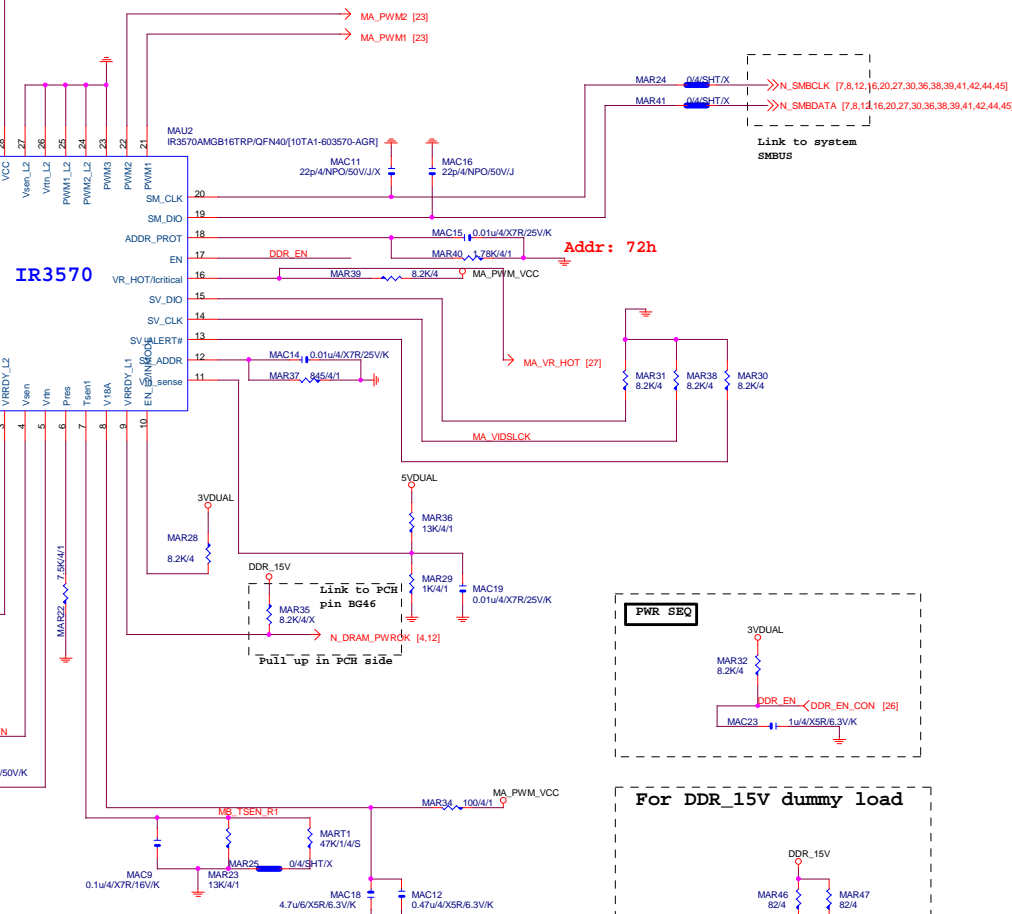
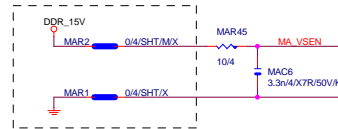
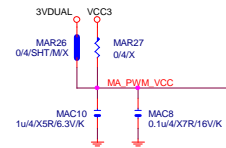
**GIGABYTE™**

Title		
HD AUDIO ALC1150		
Size	Document Number	Rev
Custom	GA-Z97X-Gaming GT	1.0
Date:	Monday, April 28, 2014	Sheet 18 of 51



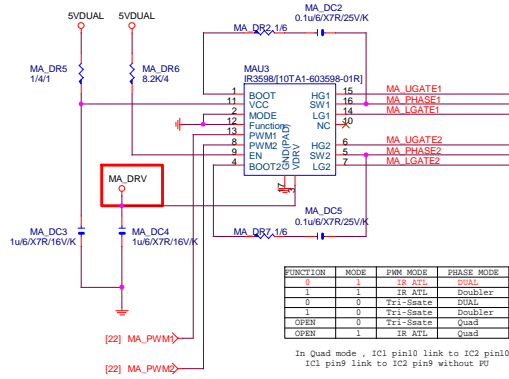






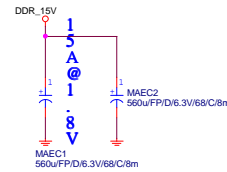
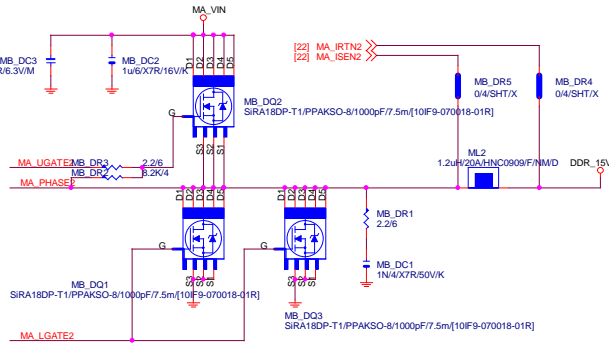
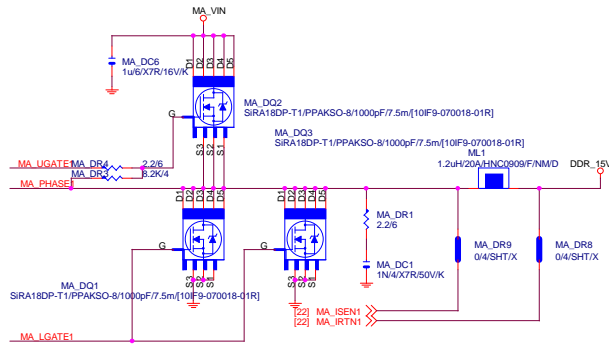
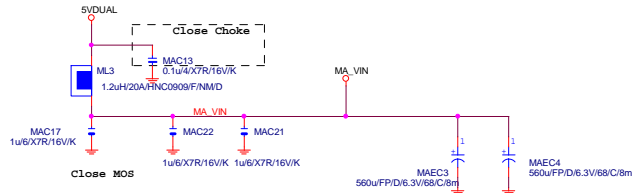


# DDR\_15V



FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	Dual
0	0	Tri-State	DUAL
1	0	Tri-State	Doubler
OPEN	0	Tri-State	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU



Gigabyte Technology

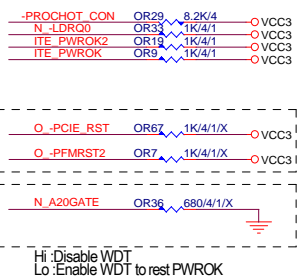
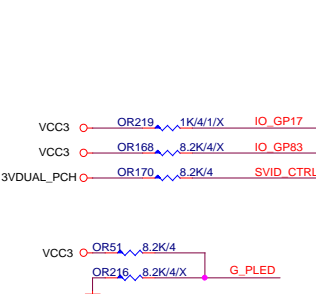
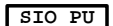
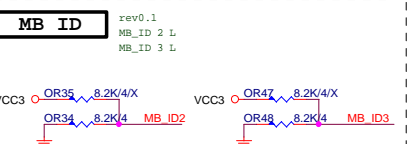
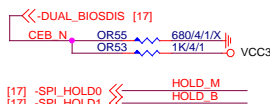
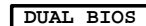
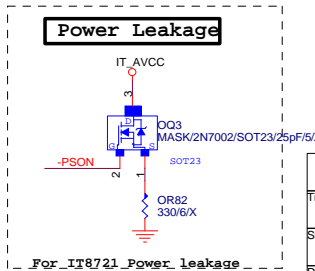
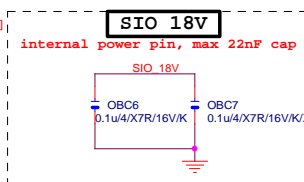
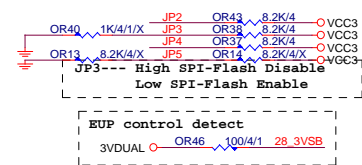
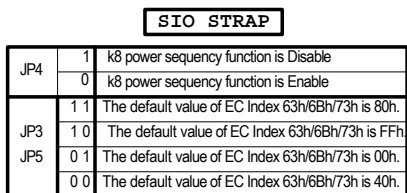
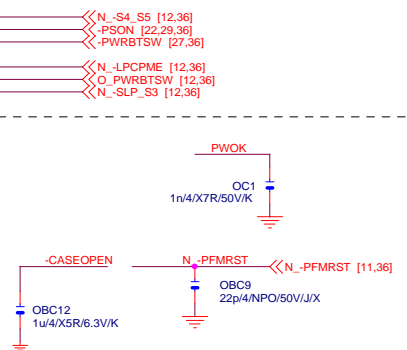
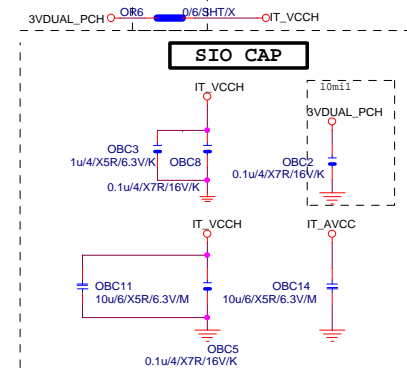
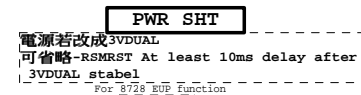
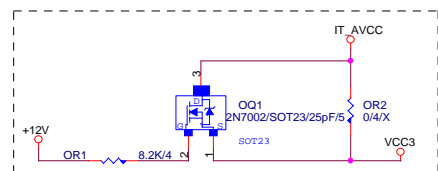
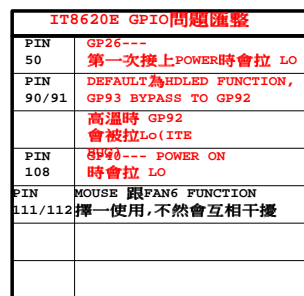
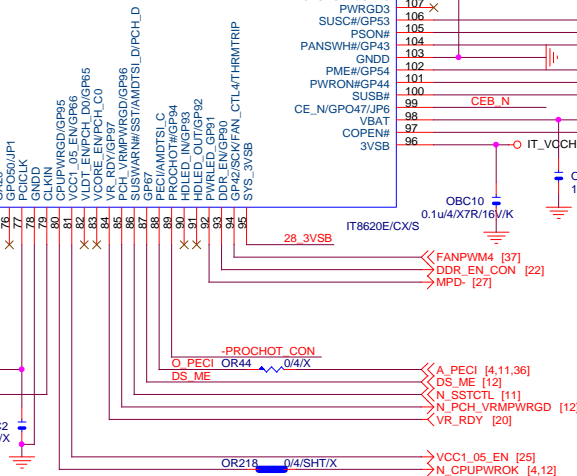
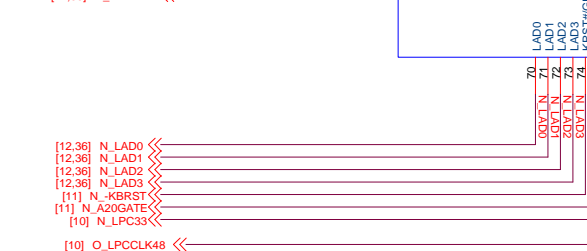
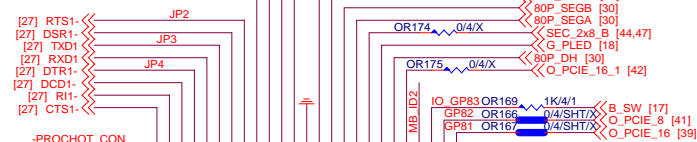
Title	IR3570
Size	Document Number
C	GA-Z97X-Gaming GT
Date	Monday, April 28, 2014
Sheet	23 of 51

5VDUAL

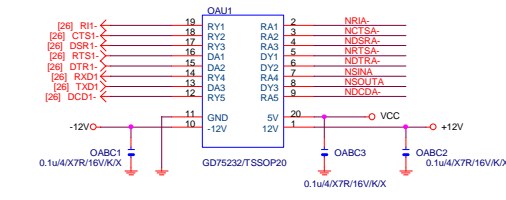
Gigabyte Technology		
Title		
DISCRETE POWER 1		
Size	Document Number	Rev
C	GA-Z97X-Gaming GT	1.0
Date:	Monday, April 28, 2014	Sheet 24 of 51



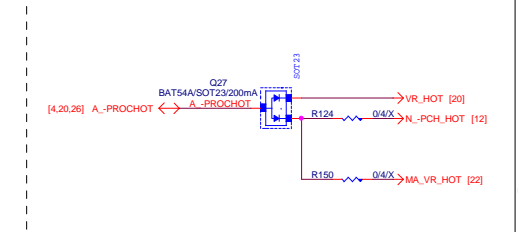
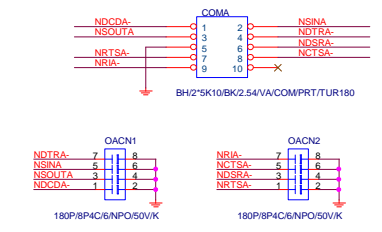
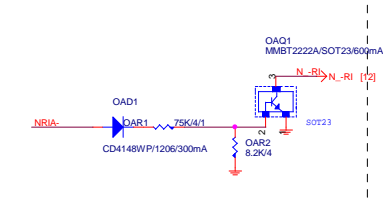
Gigabyte Technology		
File	DISCRETE POWER 2	
Size	Document Number	Rev
C	GA-Z97X-Gaming GT	1.0
Date:	Monday, April 28, 2014	Sheet 25 of 51



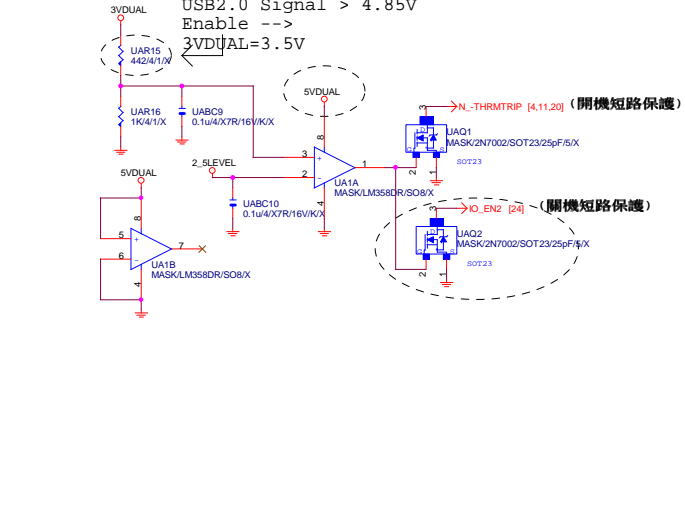
# COMA



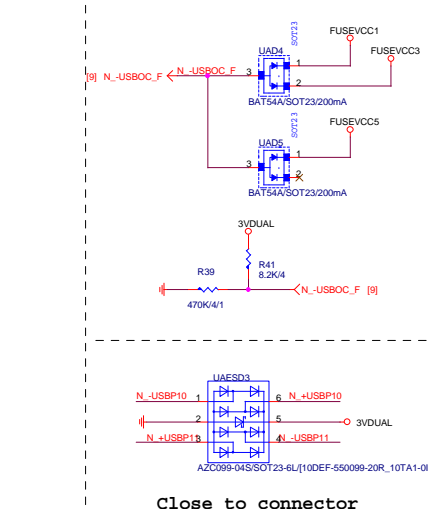
# COM RI



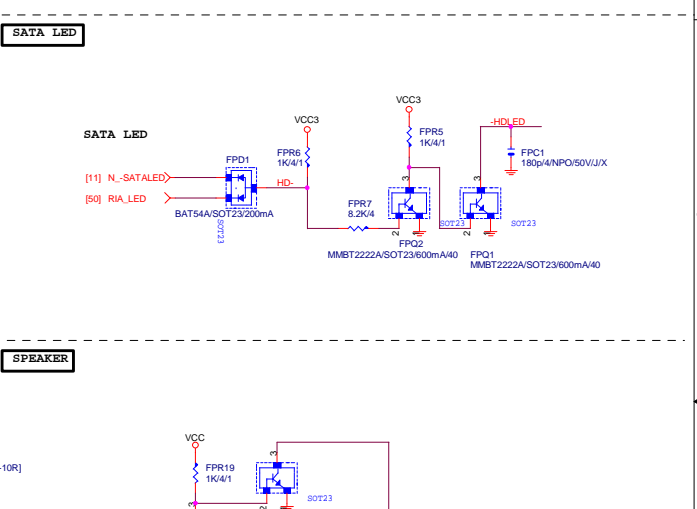
# USB2.0 Signal & power short protection



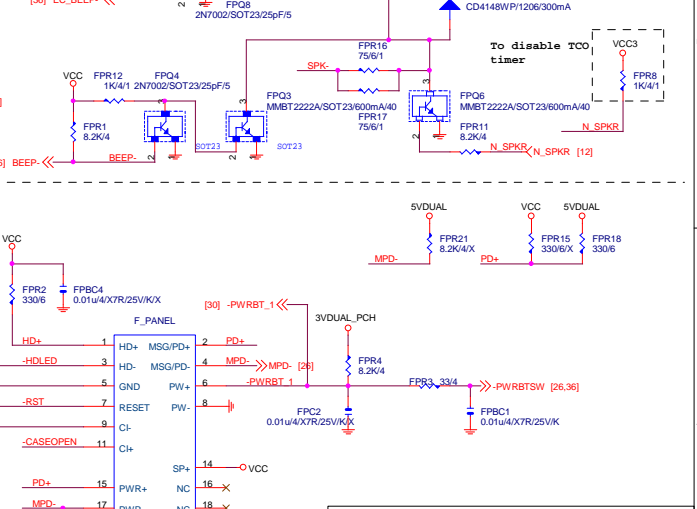
# Case Open



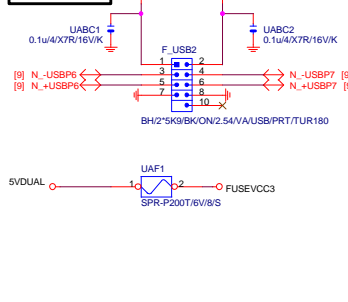
# SATA LED



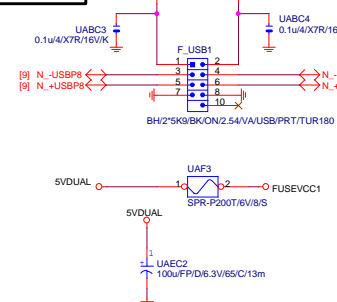
# Speaker



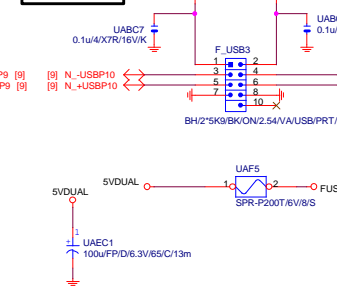
# FRONT USB2



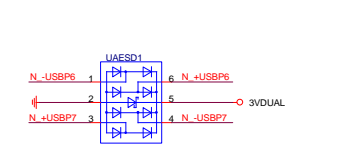
# FRONT USB1



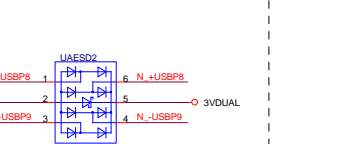
# FRONT USB3



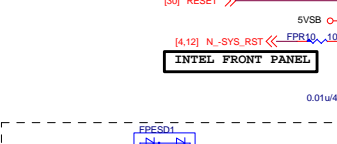
# Close to connector



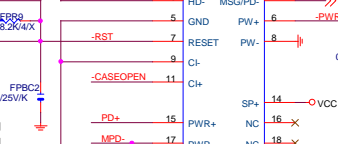
# Close to connector



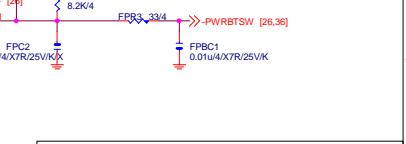
# Close to connector

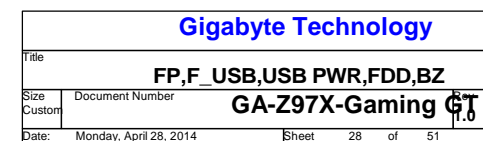
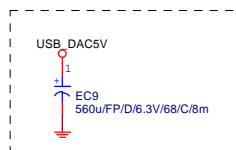
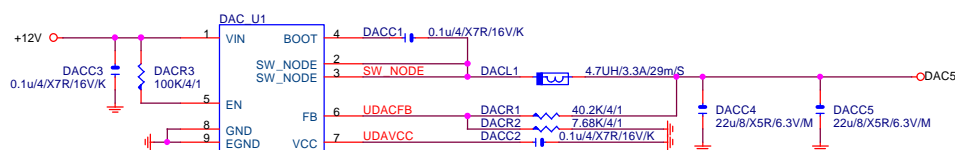
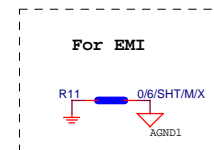
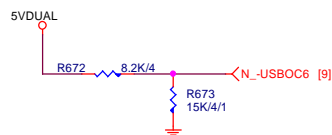


# INTEL FRONT PANEL

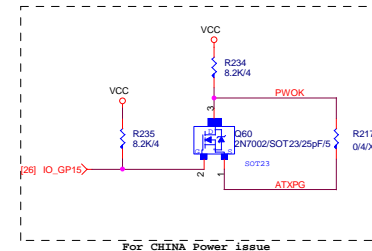
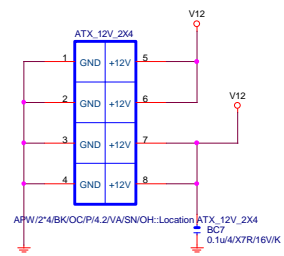


# Close to connector





## Title R&amp;D 155

[illegible]

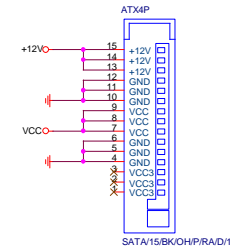
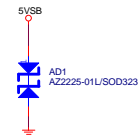
The schematic diagram illustrates the power supply circuit for the AD9288. It shows several power planes and their connections to the AD9288 pins. The components and their values are as follows:

- VOCORE:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR73 (8.2K/4/1), OC8 (1u4/XSR/6.3V/K), OC13 (1u4/XSR/6.3V/K), OC10 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).
- DDR\_15V:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR72 (8.2K/4/1), OC8 (1u4/XSR/6.3V/K), OC13 (1u4/XSR/6.3V/K), OC10 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).
- VOC3:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR8 (6.49K/4/1), OC13 (1u4/XSR/6.3V/K), OC10 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).
- +12V:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR79 (75K/4/1), OC13 (1u4/XSR/6.3V/K), OC10 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).
- CPU\_VAUXG:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR74 (8.2K/4/1), OC10 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).
- VCC:** Connected to VIN5, VIN6, VIN2, VIN4, and VIN0. Components include OR78 (15K/4/1), OC12 (1u4/XSR/6.3V/K), and OC3 (1u4/XSR/6.3V/K).

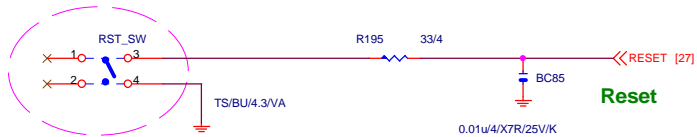
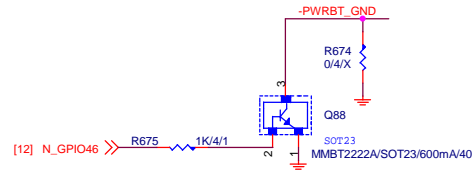
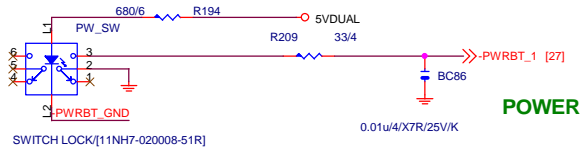
The diagram also shows the connection of the AD9288 pins to the power planes. The pins are labeled VIN5, VIN6, VIN2, VIN4, VIN3, and VIN0. The connections are as follows:

- VIN5: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.
- VIN6: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.
- VIN2: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.
- VIN4: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.
- VIN3: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.
- VIN0: Connected to VOCORE, DDR\_15V, VOC3, +12V, CPU\_VAUXG, and VCC.

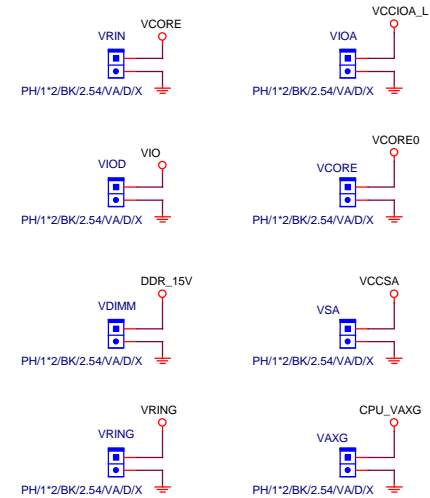
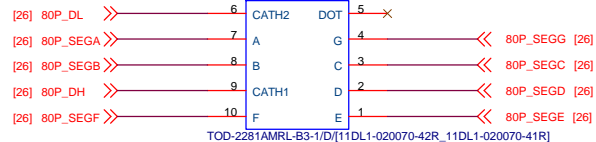
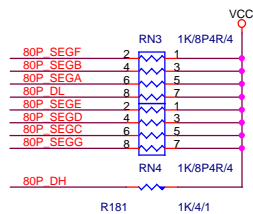
The division voltage of VIN2 & VIN3 must be around 2.9V



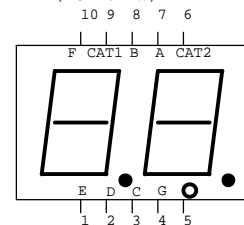




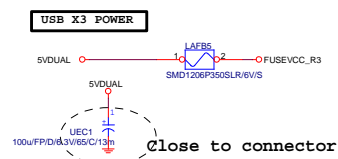
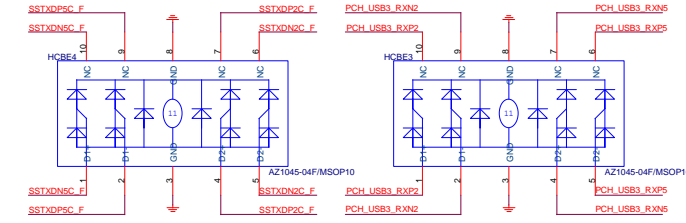
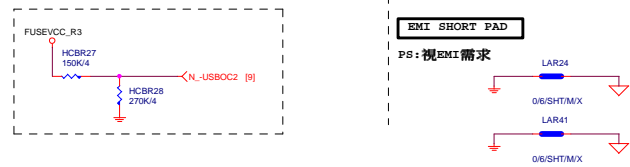
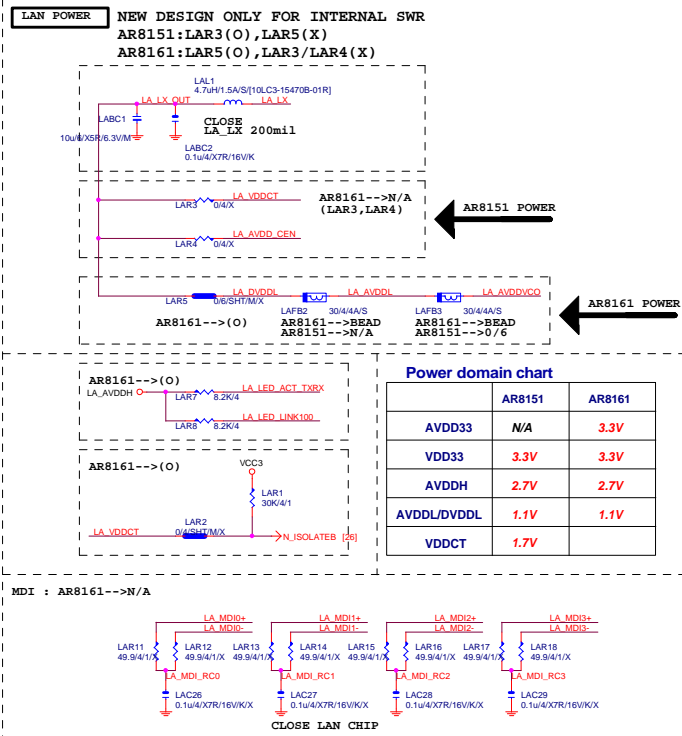
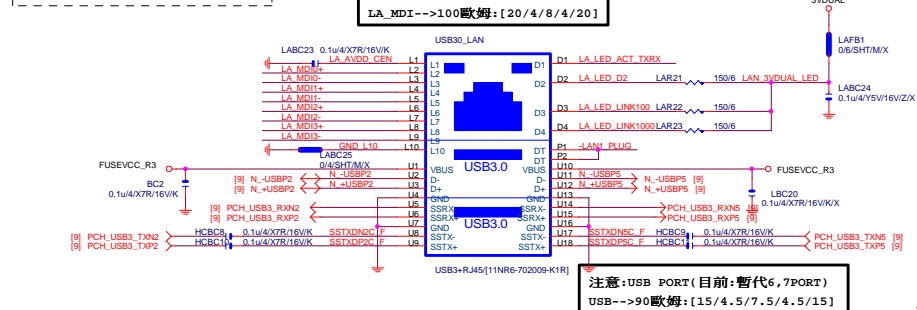
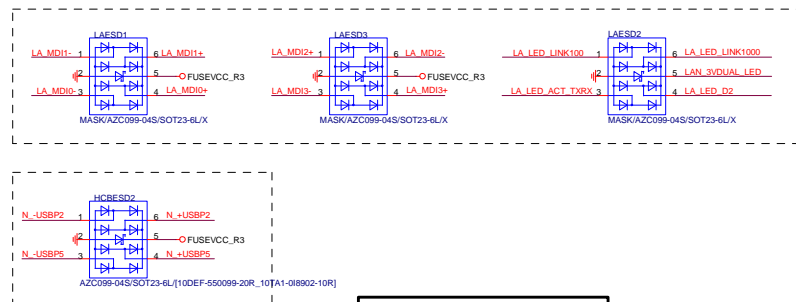
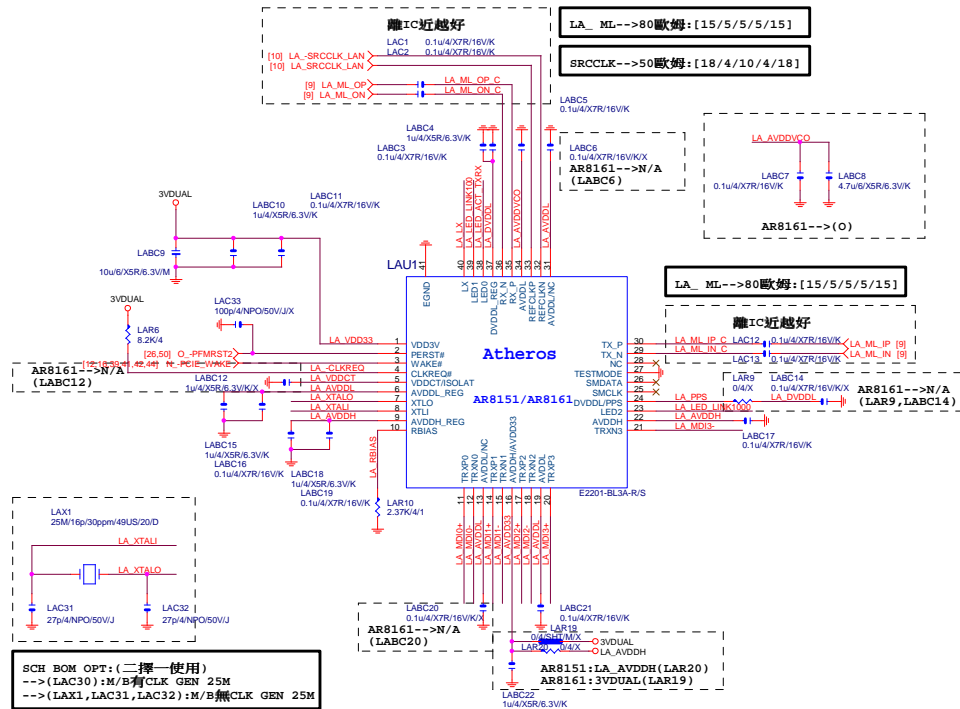
80 PORT



Physical Package  
(TOP VIEW)

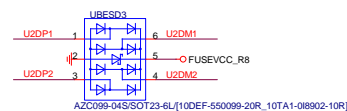
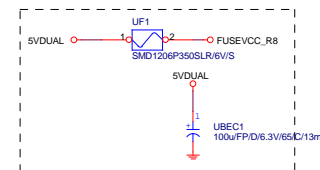
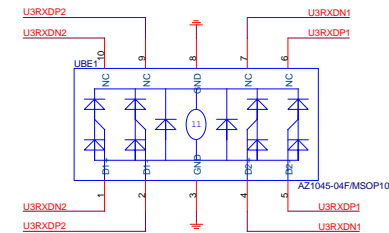
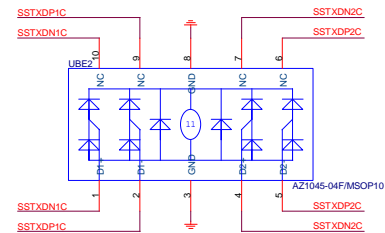
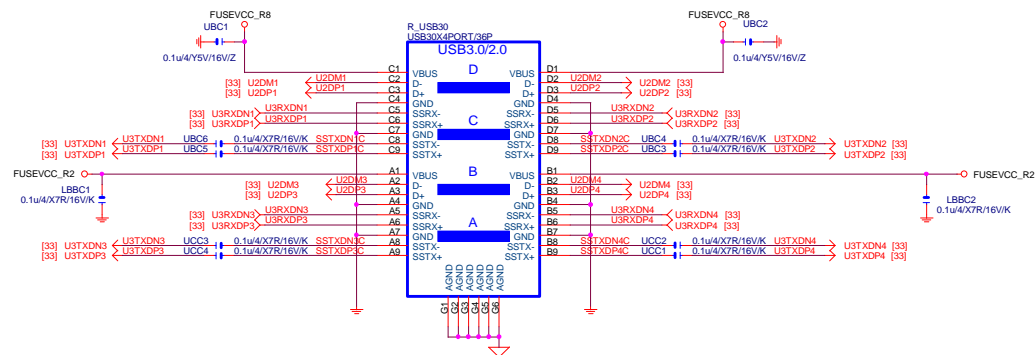


GIGABYTE™			
Title			
RST, PWR, CLR_CMOS			
Size	Document Number	Rev	
Custom	GA-Z97X-Gaming GT	1.0	
Date:	Monday, April 28, 2014	Sheet	30 of 51

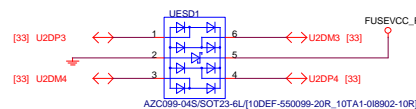
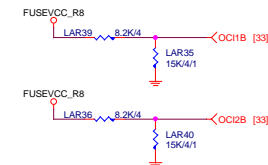


<b><i>Gigabyte Technology</i></b>			
Title <b>INTEL LAN - i210</b>			
Size Custom	Document Number <b>GA-Z97X-Gaming GT</b>	Rev <b>1.0</b>	
Date:	Monday, April 28, 2014	Sheet	31 of 51

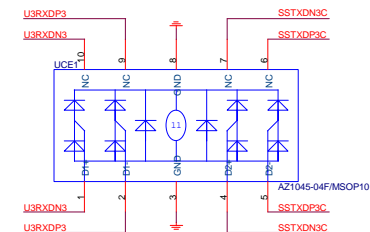
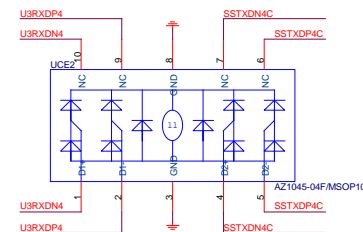
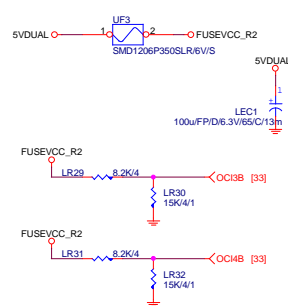
# R\_USB30 PORT



Close to connector



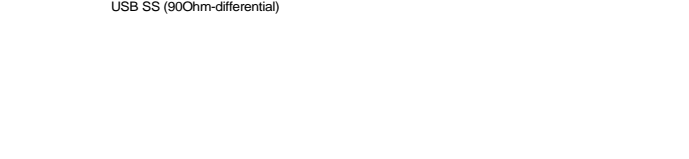
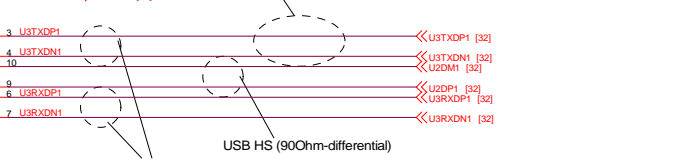
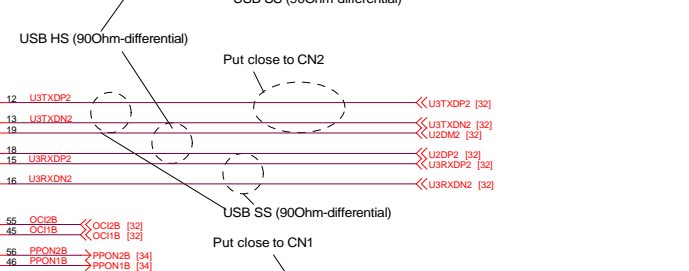
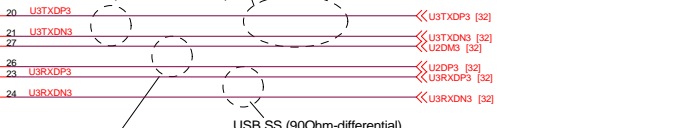
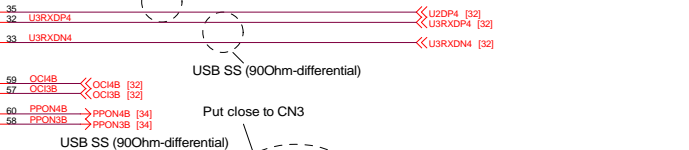
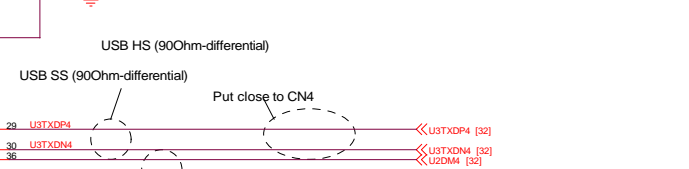
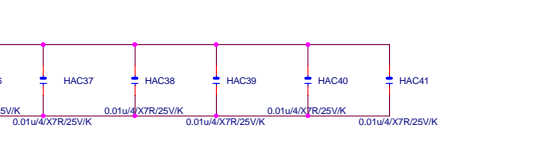
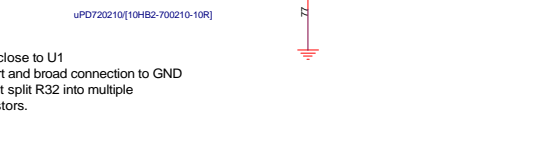
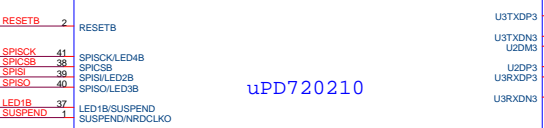
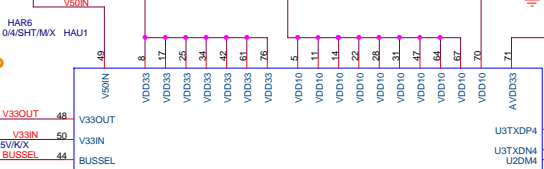
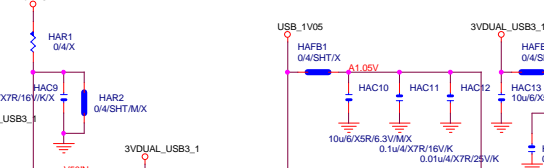
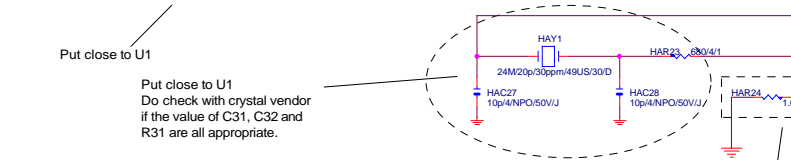
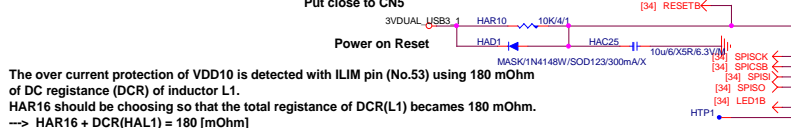
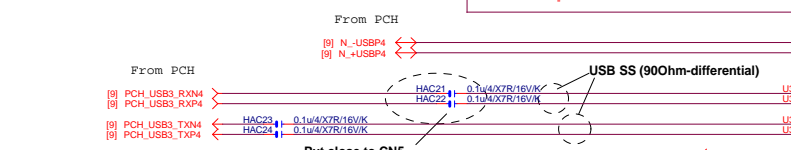
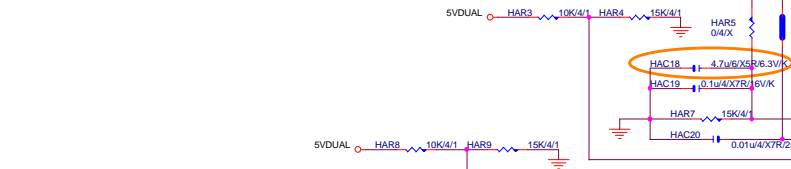
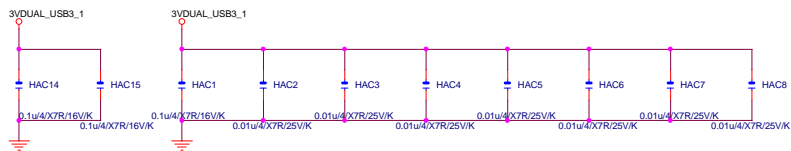
Close to connector



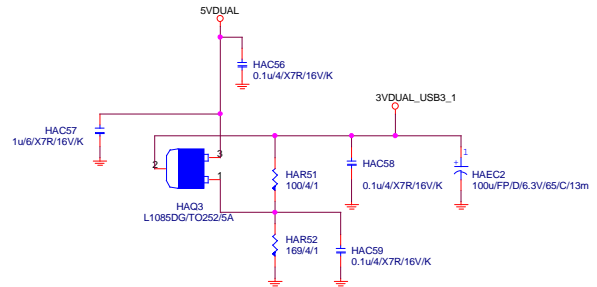
Gigabyte Technology

Title			R_USB30
Size	Document Number	GA-Z97X-Gaming GT	
Date	Monday, April 28, 2014	Sheet	32 of 51

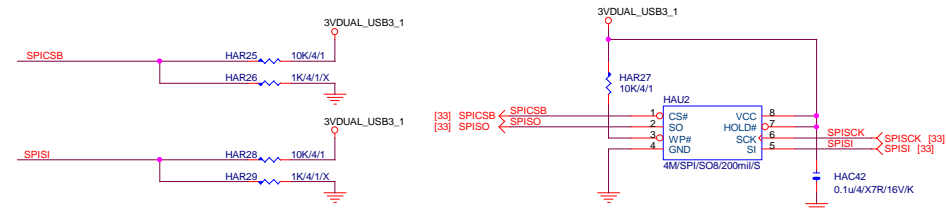
Rev 1.0



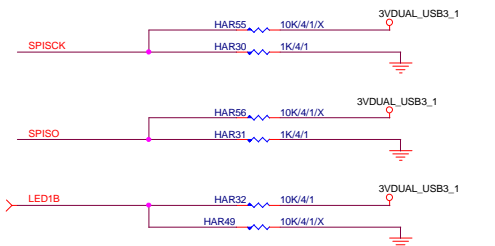
# 3VDUAL\_USB



## # External SPI ROM ; SPI ROM attached mode

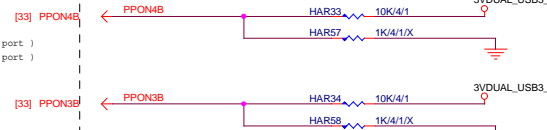


## # Battery Charging



## # Number of Ports ; 4Ports mode

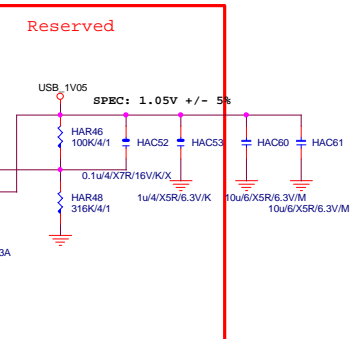
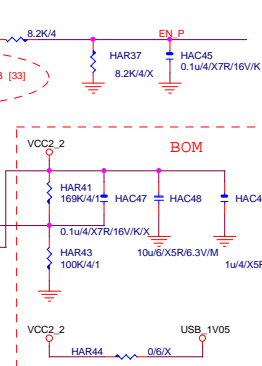
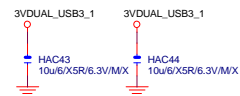
PPON3B / PPON4B : H / H ( 4 port )  
PPON3B / PPON4B : L / L ( 2 port )



## #5 VBUS Power Control ; Individual mode



## # PPON1B Pin Function ; Port1 PPONB mode



Reserved

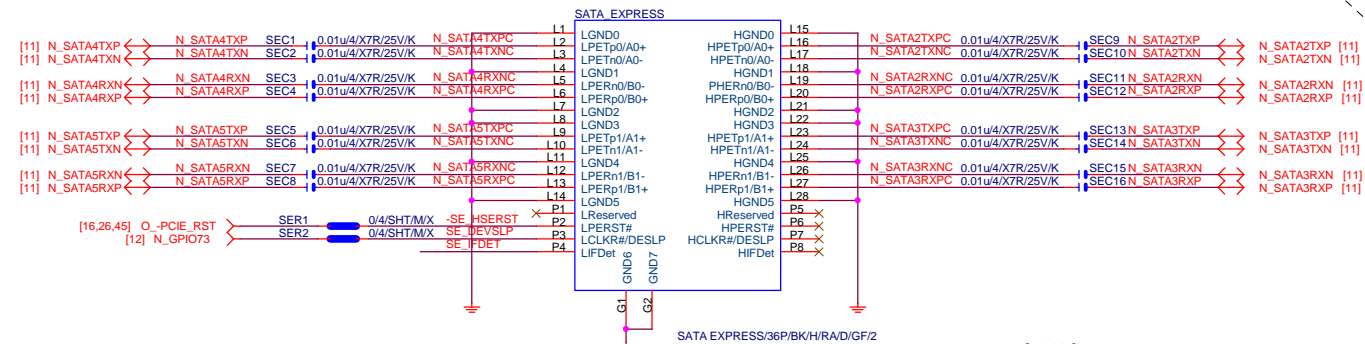
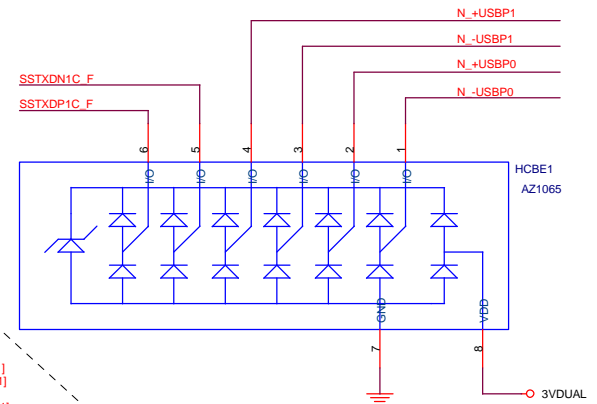
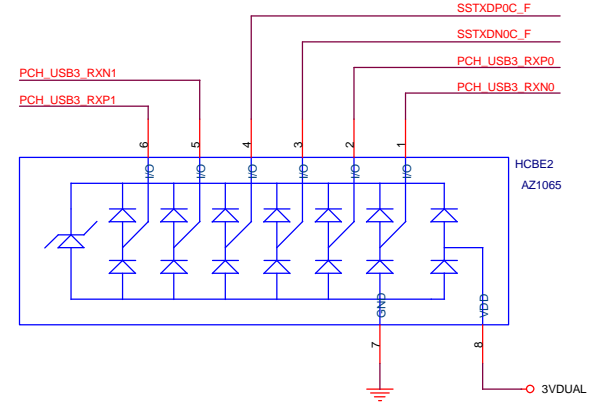
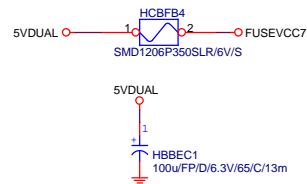
RESETB [33]

RESETB [33]

RESETB [33]

**GIGABYTE**

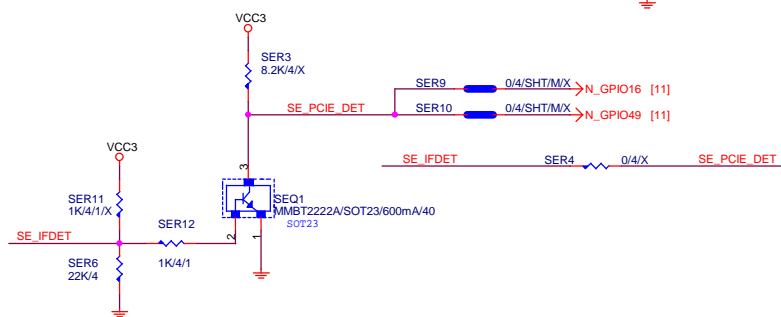
Title		
D720210 4port Hub		
Size	Document Number	Rev
Custom	GA-Z97X-Gaming GT	1.0
Date	Monday, April 28, 2014	Sheet 34 of 51

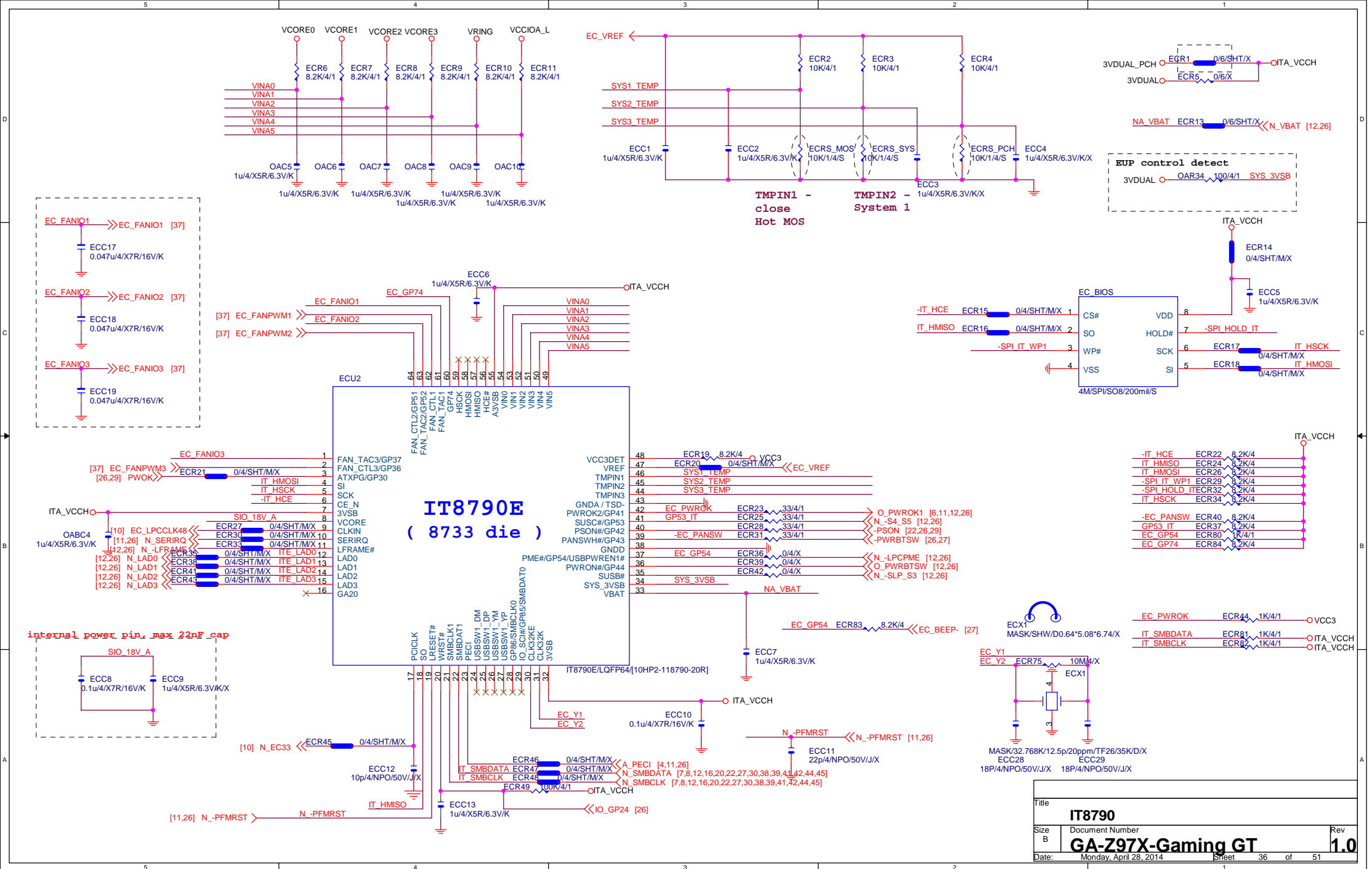


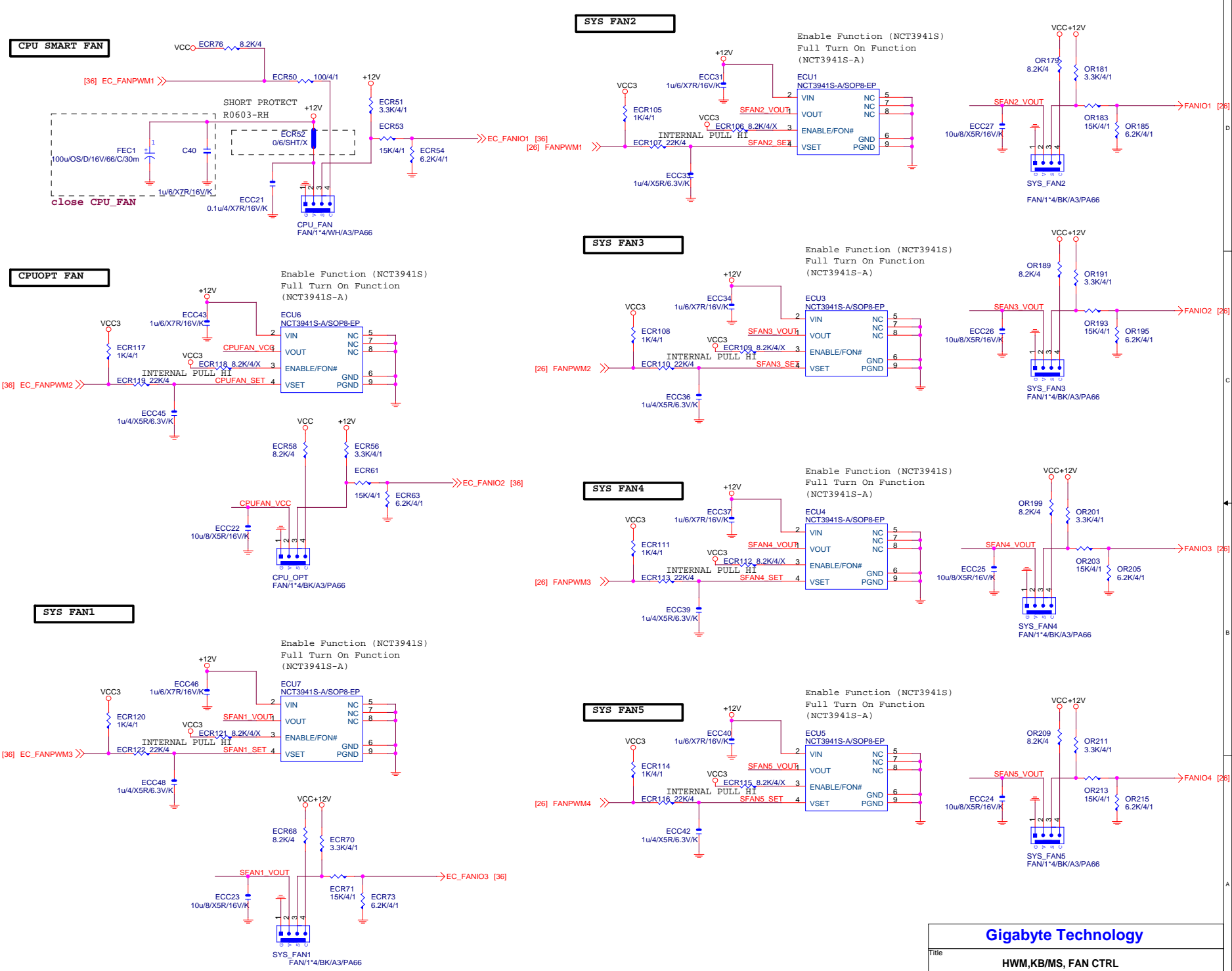
SATA EXPRESS料號

**雙層:11NR6-C10236-03R**

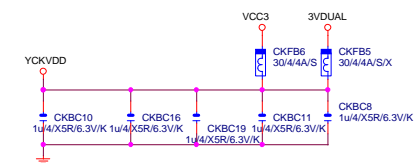
單層:11NR6-C10118-01R

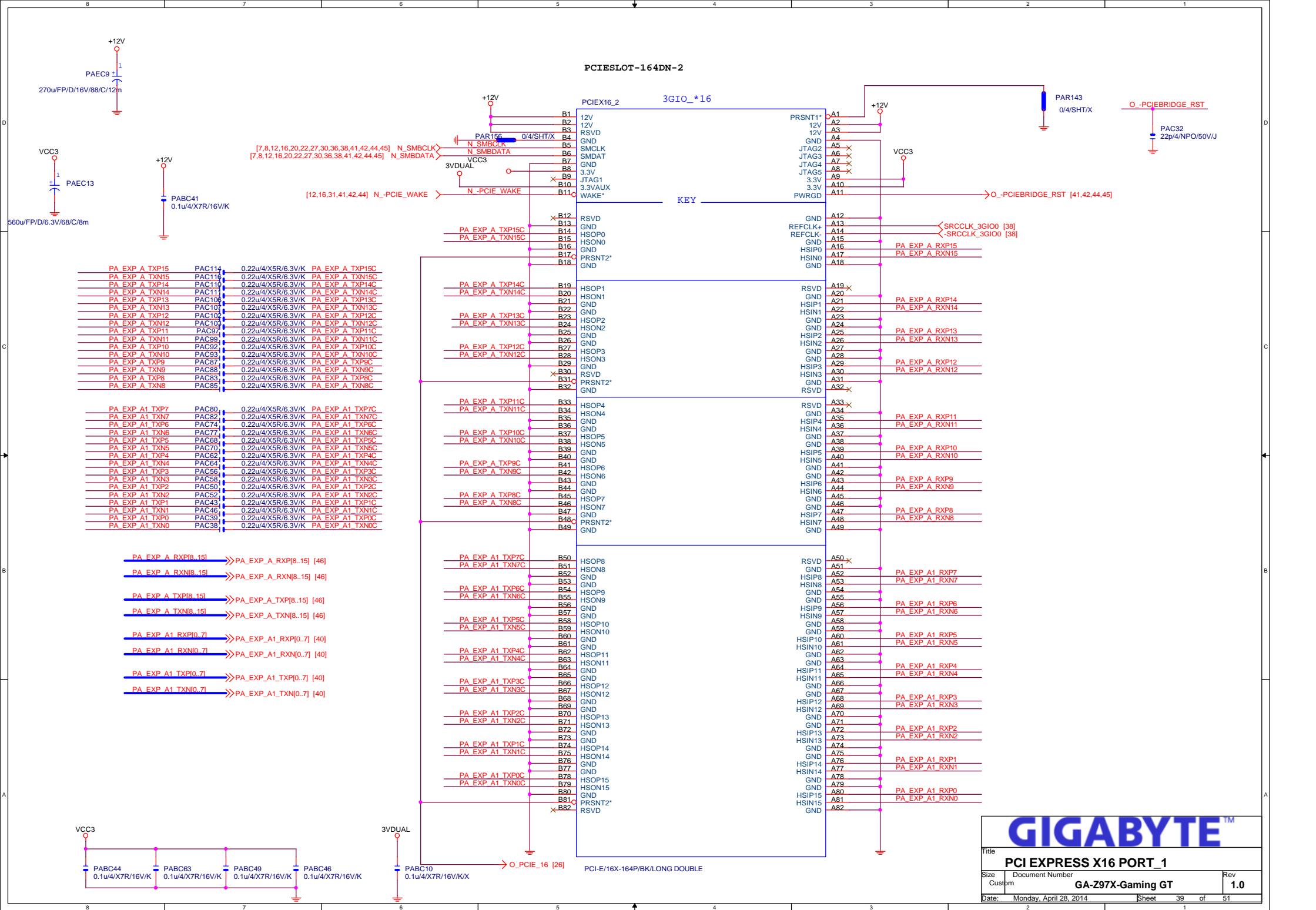


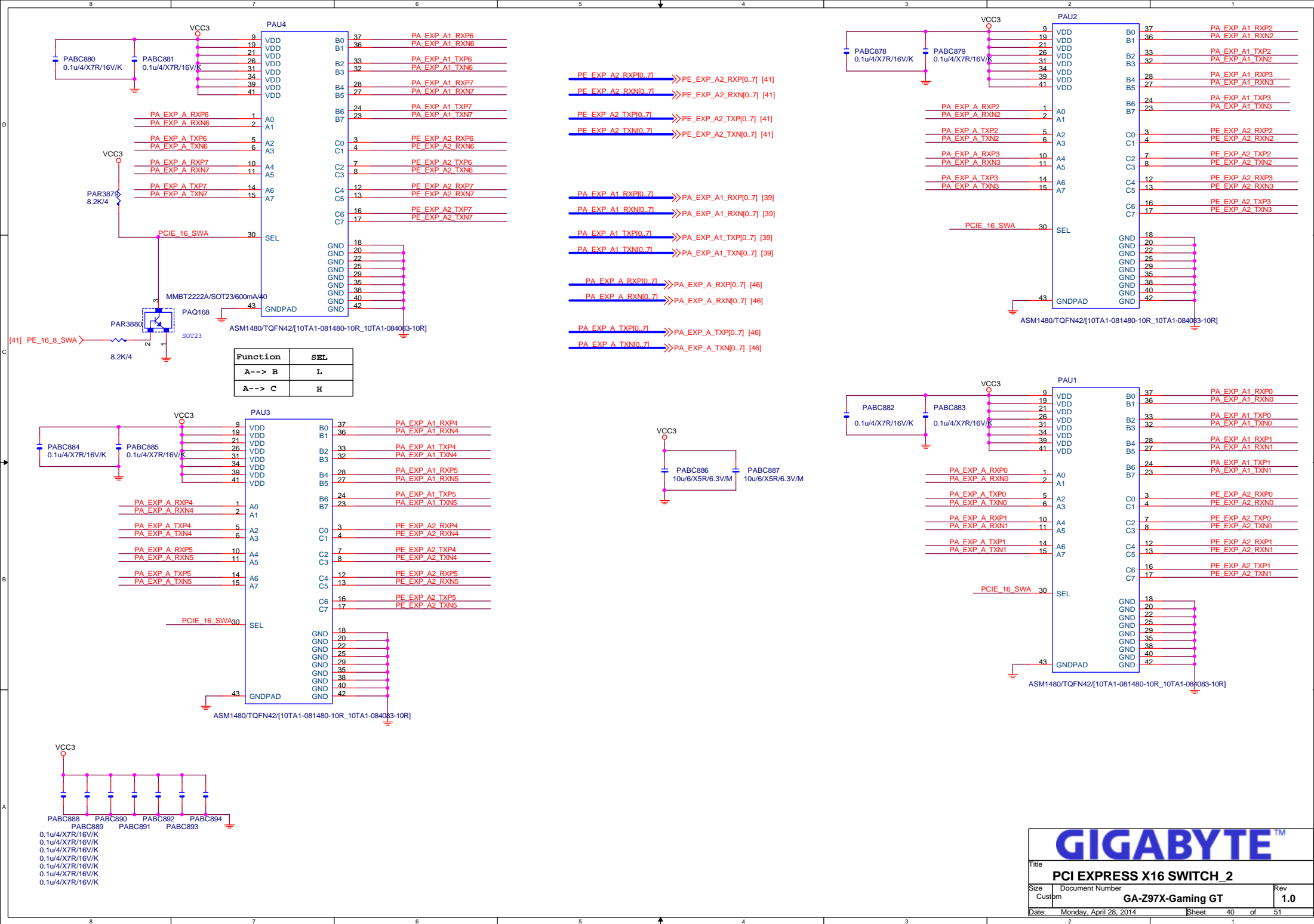


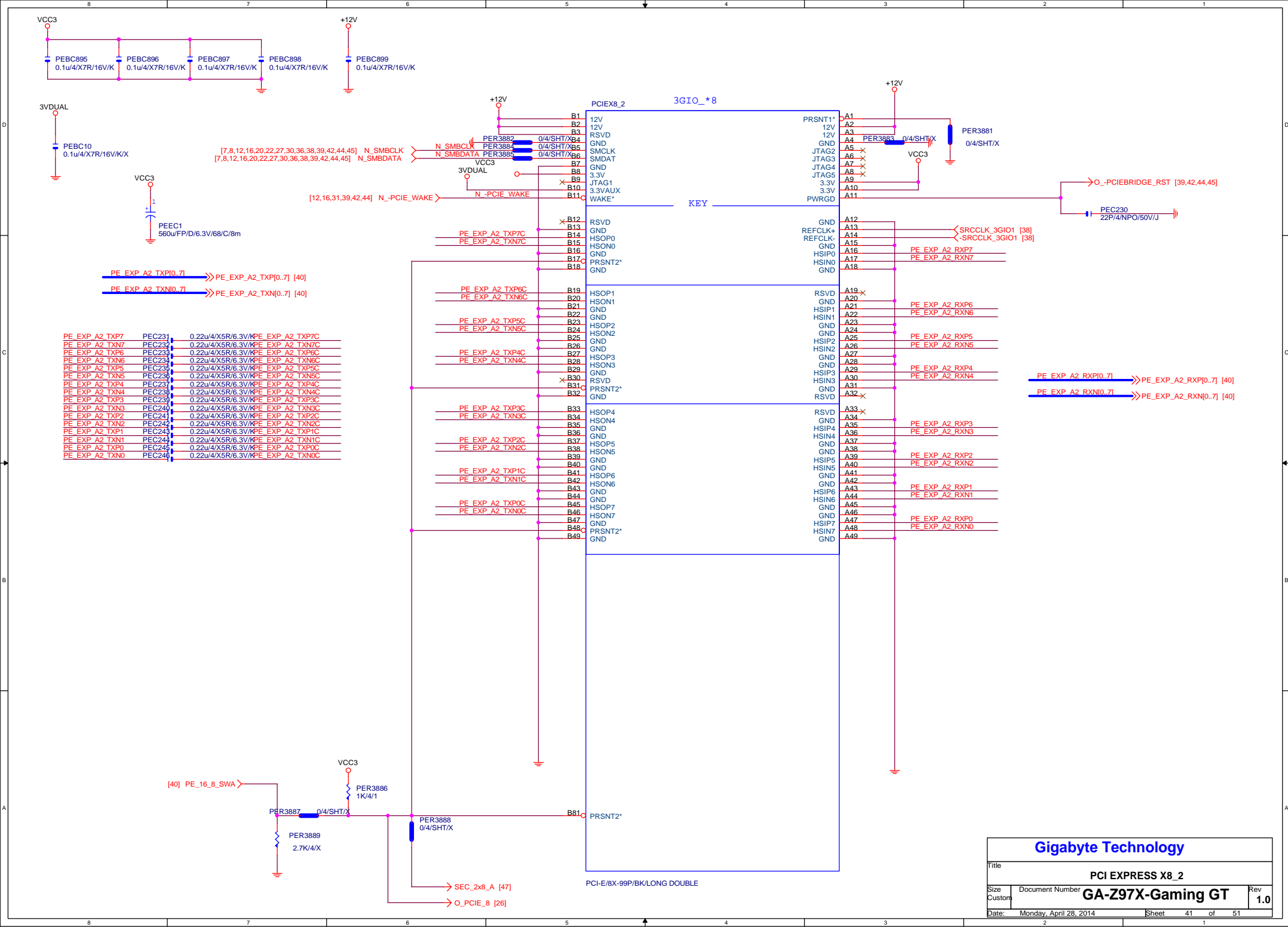


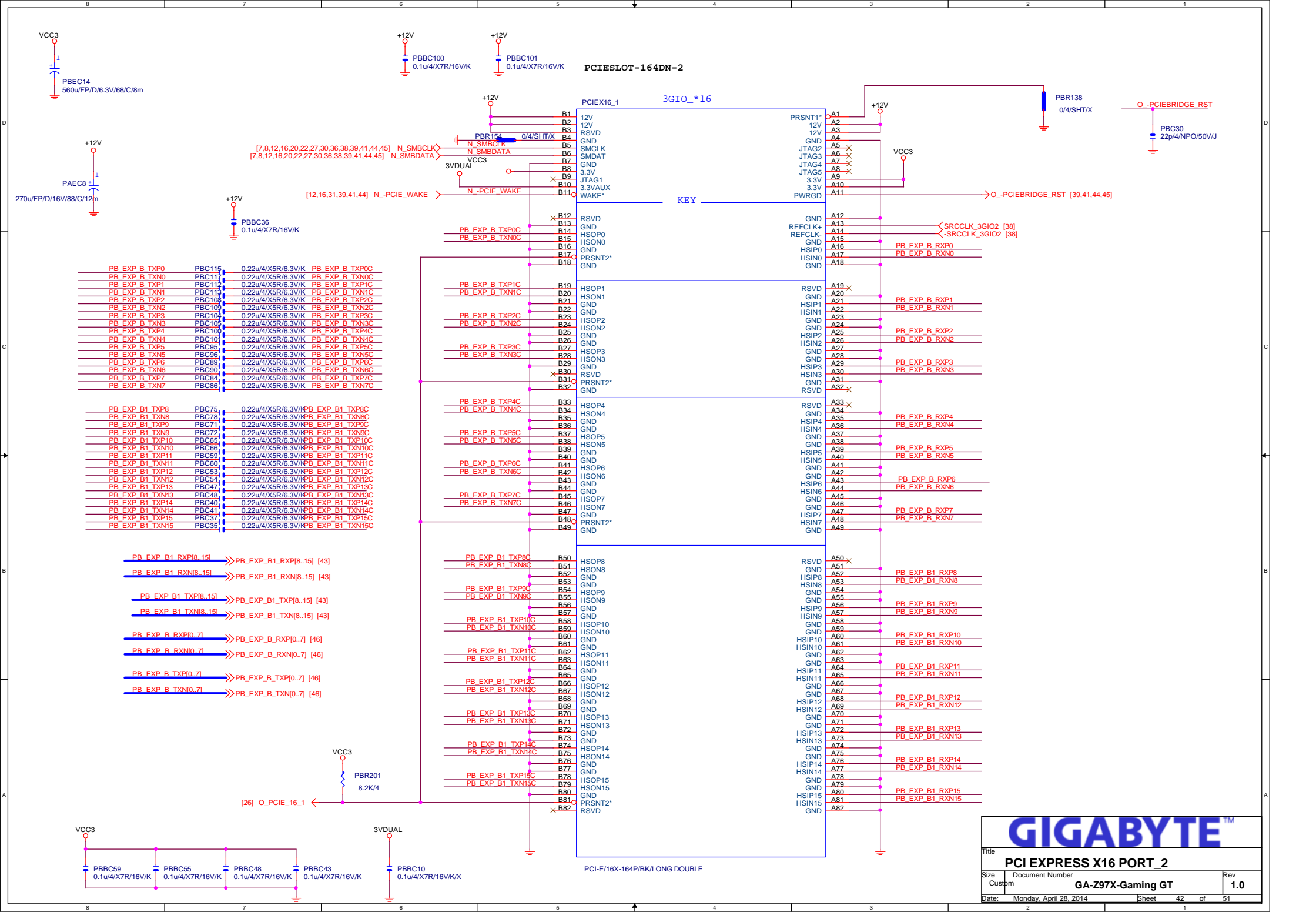


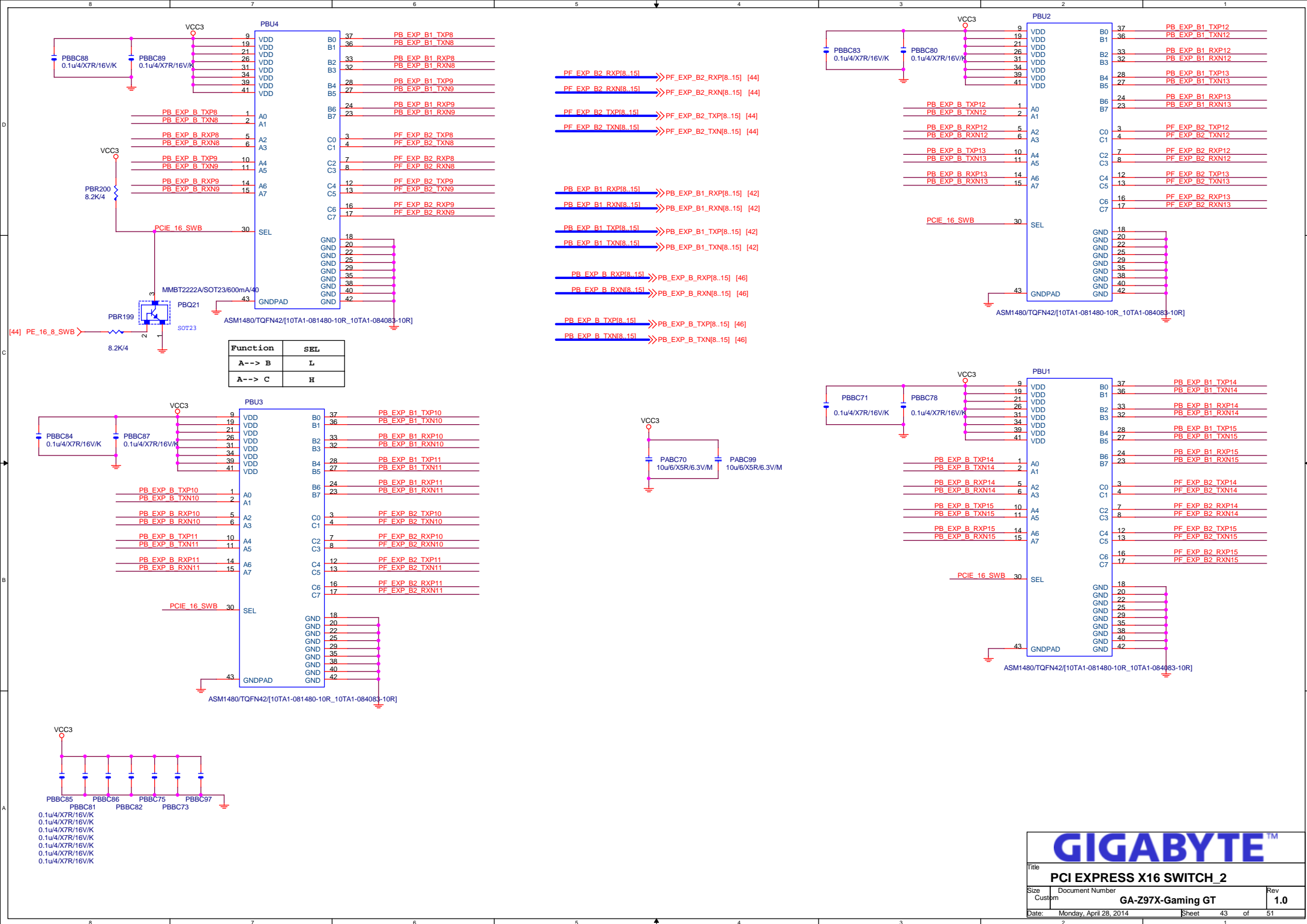


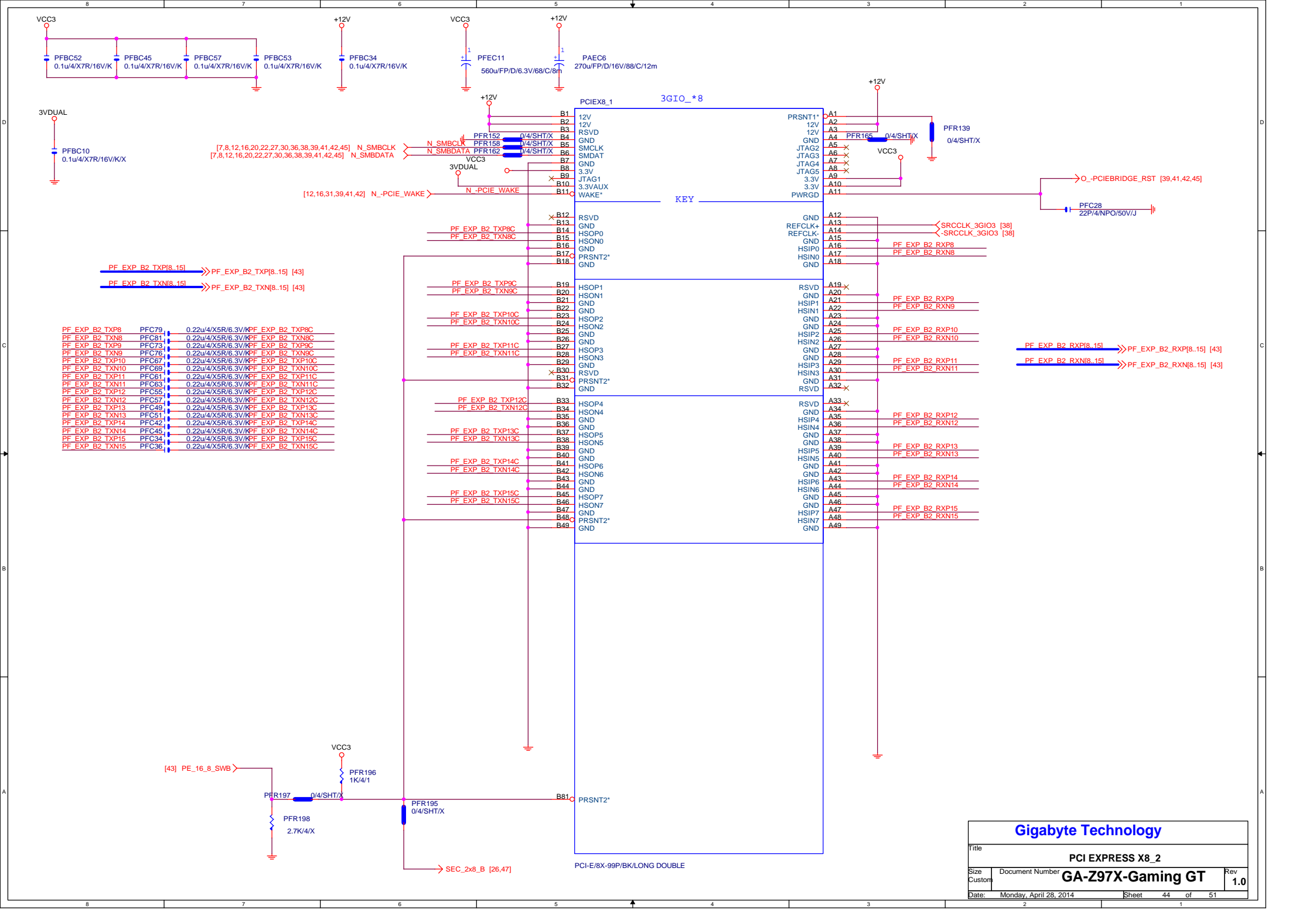




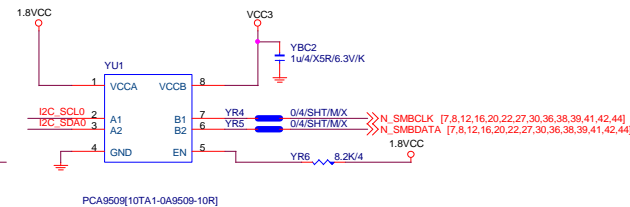
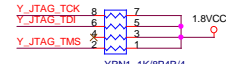
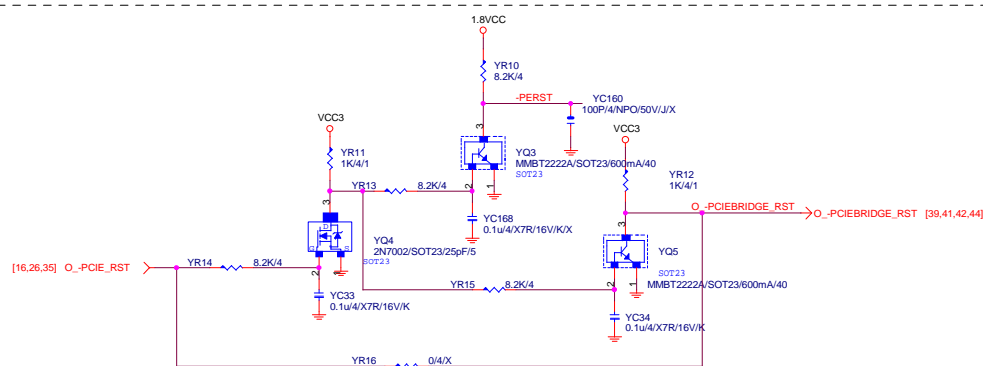
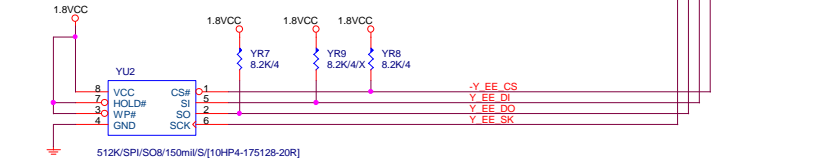
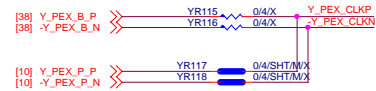
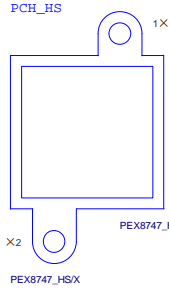








PY\_EXP\_A\_TXP0\_15I >>> PY\_EXP\_A\_TXP0\_15 [4]  
PY\_EXP\_A\_TXN0\_15I >>> PY\_EXP\_A\_TXN0\_15 [4]  
PY\_EXP\_RXP0\_15I >>> PY\_EXP\_RXP0\_15 [4]  
PY\_EXP\_RXN0\_15I >>> PY\_EXP\_RXN0\_15 [4]



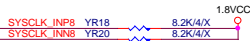


USB			
PA EXP A RXP0	V4	PEX_PETP16	V2
PA EXP A RXN0	V5	PEX_PERN16	V1
PA EXP A RXP1	U4	PEX_PETP17	U2
PA EXP A RXN1	U5	PEX_PETP17	U1
PA EXP A RXP2	R5	PEX_PETN17	R2
PA EXP A RXN2	R4	PEX_PETP18	R1
PA EXP A RXP3	P5	PEX_PETN18	P2
PA EXP A RXN3	P4	PEX_PETP19	P1
PA EXP A RXP4	M5	PEX_PETN19	M2
PA EXP A RXN4	M4	PEX_PETP20	M1
PA EXP A RXP5	L5	PEX_PETN20	L2
PA EXP A RXN5	L4	PEX_PETP21	L1
PA EXP A RXP6	J5	PEX_PETN21	J2
PA EXP A RXN6	J4	PEX_PETP22	J1
PA EXP A RXP7	H5	PEX_PETP23	H2
PA EXP A RXN7	H4	PEX_PETN23	H1
PA EXP A RXP8	D1	PEX_PETP24	A1
PA EXP A RXN8	D2	PEX_PETN24	A2
PA EXP A RXP9	E4	PEX_PETP25	B4
PA EXP A RXN9	E5	PEX_PETN25	B5
PA EXP A RXP10	D4	PEX_PETP26	A4
PA EXP A RXN10	D5	PEX_PETN26	A5
PA EXP A RXP11	E7	PEX_PETP27	B7
PA EXP A RXN11	E8	PEX_PETN27	B8
PA EXP A RXP12	D7	PEX_PETP28	A7
PA EXP A RXN12	D8	PEX_PETN28	A8
PA EXP A RXP13	E10	PEX_PETP29	B10
PA EXP A RXN13	E11	PEX_PETN29	B11
PA EXP A RXP14	D10	PEX_PETP30	A10
PA EXP A RXN14	D11	PEX_PETN30	A11
PA EXP A RXP15	E11	PEX_PETP31	A11
PA EXP A RXN15	D11	PEX_PETN31	A11
PB EXP B RXP0	V19	PEX_PETP32	V22
PB EXP B RXN0	V20	PEX_PETN32	V23
PB EXP B RXP1	U19	PEX_PETP33	U22
PB EXP B RXN1	U20	PEX_PETN33	U23
PB EXP B RXP2	R19	PEX_PETP34	R22
PB EXP B RXN2	R20	PEX_PETN34	R23
PB EXP B RXP3	P19	PEX_PETP35	P22
PB EXP B RXN3	P20	PEX_PETN35	P23
PB EXP B RXP4	M19	PEX_PETP36	M22
PB EXP B RXN4	M20	PEX_PETN36	M23
PB EXP B RXP5	L19	PEX_PETP37	L22
PB EXP B RXN5	L20	PEX_PETN37	L23
PB EXP B RXP6	J19	PEX_PETP38	J22
PB EXP B RXN6	J20	PEX_PETN38	J23
PB EXP B RXP7	H19	PEX_PETP39	H22
PB EXP B RXN7	H20	PEX_PETN39	H23
PB EXP B RXP8	E23	PEX_PETP40	B23
PB EXP B RXN8	E22	PEX_PETN40	B22
PB EXP B RXP9	D22	PEX_PETP41	A22
PB EXP B RXN9	D20	PEX_PETN41	A20
PB EXP B RXP10	E20	PEX_PETP42	B20
PB EXP B RXN10	D20	PEX_PETN42	A20
PB EXP B RXP11	E19	PEX_PETP43	B19
PB EXP B RXN11	D19	PEX_PETN43	A19
PB EXP B RXP12	D17	PEX_PETP44	B17
PB EXP B RXN12	D17	PEX_PETN44	A17
PB EXP B RXP13	E16	PEX_PETP45	B16
PB EXP B RXN13	E14	PEX_PETN45	A16
PB EXP B RXP14	D14	PEX_PETP46	B14
PB EXP B RXN14	D13	PEX_PETN46	A14
PB EXP B RXP15	D13	PEX_PETP47	B13
PB EXP B RXN15	D13	PEX_PETN47	A13

SYSCLK\_INP4 P7  
SYSCLK\_INN4 P6

PEX8747SABOFBCBGEGA67S[10TA1-09874-20R]

P17 SYSCLK\_INP8  
P18 SYSCLK\_INN8



NOT INSTALL

PA EXP A RXP[0..7] >>> PA\_EXP\_A\_RXP[0..7] [40]  
PA EXP A RXN[0..7] >>> PA\_EXP\_A\_RXN[0..7] [40]

PA EXP A TXP[0..7] >>> PA\_EXP\_A\_TXP[0..7] [40]  
PA EXP A TXN[0..7] >>> PA\_EXP\_A\_TXN[0..7] [40]

PA EXP A RXP[8..15] >>> PA\_EXP\_A\_RXP[8..15] [39]  
PA EXP A RXN[8..15] >>> PA\_EXP\_A\_RXN[8..15] [39]

PA EXP A TXP[8..15] >>> PA\_EXP\_A\_TXP[8..15] [39]  
PA EXP A TXN[8..15] >>> PA\_EXP\_A\_TXN[8..15] [39]

PB EXP B RXP[0..7] >>> PB\_EXP\_B\_RXP[0..7] [42]  
PB EXP B RXN[0..7] >>> PB\_EXP\_B\_RXN[0..7] [42]

PB EXP B TXP[0..7] >>> PB\_EXP\_B\_TXP[0..7] [42]  
PB EXP B TXN[0..7] >>> PB\_EXP\_B\_TXN[0..7] [42]

PB EXP B RXP[8..15] >>> PB\_EXP\_B\_RXP[8..15] [43]  
PB EXP B RXN[8..15] >>> PB\_EXP\_B\_RXN[8..15] [43]

PB EXP B TXP[8..15] >>> PB\_EXP\_B\_TXP[8..15] [43]  
PB EXP B TXN[8..15] >>> PB\_EXP\_B\_TXN[8..15] [43]

**GIGABYTE™**

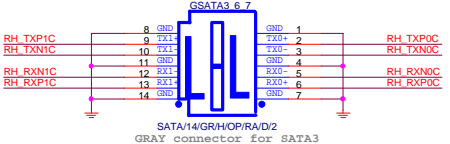
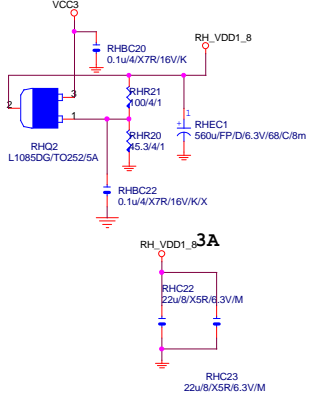
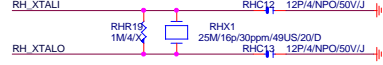
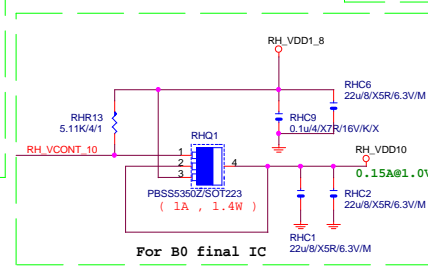
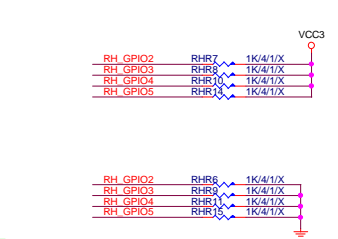
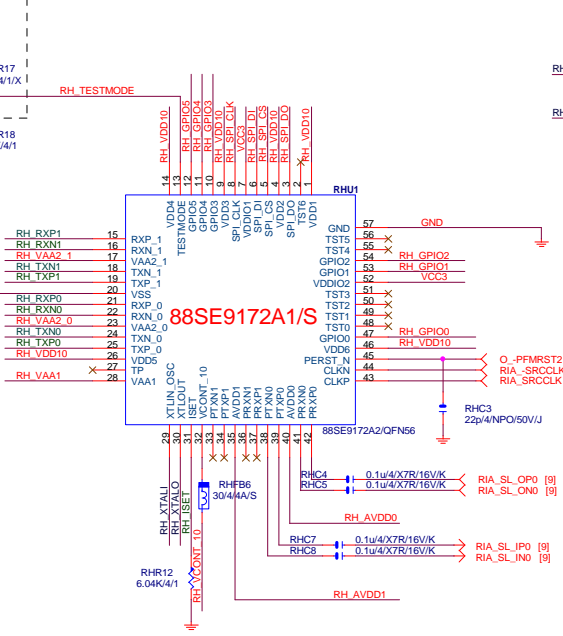
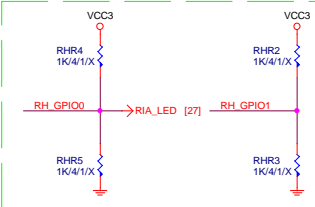
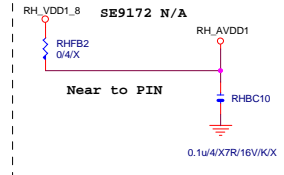
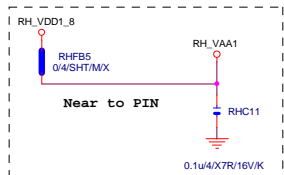
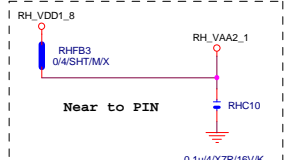
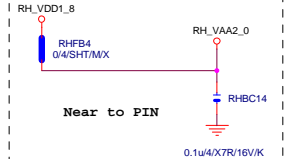
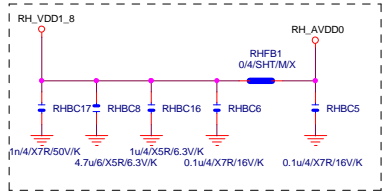
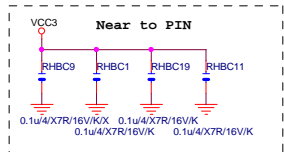
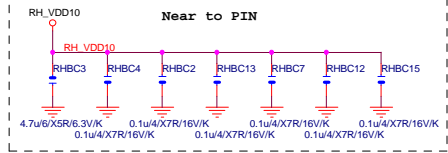
Title <b>PEX8747S DOWNSTREAM SLOTS</b>		
Size Custom	Document Number <b>GA-Z97X-Gaming GT</b>	Rev <b>1.0</b>
Date: Monday, April 28, 2014 Sheet 46 of 51		







Title			
<b>PEX8747 POWER DESIGN</b>			
Size	Document Number	Rev	
Custom	<b>GA-Z97X-Gaming GT</b>	<b>1.0</b>	
Date:	Monday, April 28, 2014	Sheet	49 of 51



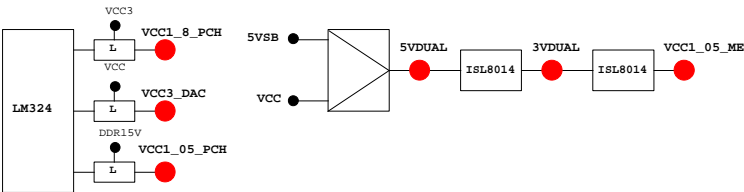
灰色 connector

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKT0CC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	

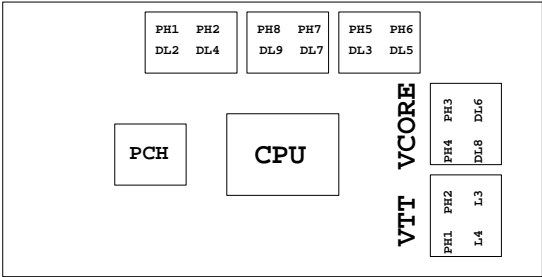
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMB_D_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMB_D_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
Title	TABLE LIST		
Size C	Document Number	GA-Z97X-Gaming GT	Rev 1.0
Date:	Monday, April 28, 2014	Sheet 51	of 51